CS3400 - Principles of Software Engineering
Software Engineering for Multicore Systems

V. Krishna Nandivada

IBM Research - India
Part I

Patterns
A pattern language for parallel programs

Structure the given problem to expose exploitable concurrency.

Structuring the algorithm to take advantage of potential concurrency.

Helps algorithm to be implemented.

How the high level specifications are mapped.

Goal: Identify patterns in each stage.
Overall big picture

Finding Concurrency

Algorithm Structure

Units of execution + new shared data for extracted dependencies

Supporting struct. & impl. mech.

Tasks, shared and local data

Corresponding source code
Finding concurrency and Algorithm Structure

- Decomposition
  - Task Decomposition
  - Data Decomposition

- Dependency Analysis
  - Group Tasks
  - Order Tasks
  - Data Sharing

Design Evaluation

Organize By Tasks
- Task Parallelism
- Divide and Conquer

Organize By Data Decomposition
- Geometric Decomposition
- Recurse Data

Organize By Flow of Data
- Pipeline
- Event-Based Coordination

Supporting Structures

Program Structures
- SPMD
- Master/Worker
- Loop Parallelism
- Fork/Join

Data Structures
- Shared Data
- Shared Queue
- Distributed Array

Implementation Mechanisms
Implementation Mechanisms

- Finding Concurrency
- Algorithm Structure
- Supporting Structures

Implementation Mechanisms:
- UE Management
- Synchronization
- Communication
Synchronization:

Synchronization: Enforces constraint among parallel events.
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

```
done=true;
while(done) ;
done = false;
```

Value may be present in cache. Cache coherence may take care.

Value may not be read. How?

```
x = y = 0
Thread 1
Thread 2
1: r1 = x
4: x = 1
2: y = 1
r3 = y
3: r2 = x
r1 == r2 == r3 == 0. Possible?
```

V.Krishna Nandivada (IBM Research - India)
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

- done=true;
- while(done) ;
- done = false;
- Value may be present in cache.

Thread 1
1: r1 = x
Thread 2
2: y = 1
3: r2 = x
4: x = 1
r3 = y

r1 == r2 == r3 == 0. Possible?
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

- done=true;
- while(done) {
  done = false;
  Value may be present in cache. cache coherence may take care.
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

```c
done=true;
while(done) {
    done = false;
    Value may be present in cache. cache coherence may take care.
    Value may be present in a register - Culprit compiler.
}
```

Thread 1
1: r1 = x
2: y = 1
3: r2 = x
r1 == r2 == r3 == 0. Possible?
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

- done=true;
  while (done) {
  done = false;
  }

- Value may be present in cache. Cache coherence may take care.
- Value may be present in a register - Culprit compiler.
- Value may not be read. How?
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

- 

```
done=true;
while(done) ;
done = false;
```

- Value may be present in cache. cache coherence may take care.
- Value may be present in a register - Culprit compiler.
- Value may not be read. How?

- 

<table>
<thead>
<tr>
<th>Thread 1</th>
<th>Thread 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1: r1 = x</td>
<td>4: x = 1</td>
</tr>
<tr>
<td>2: y = 1</td>
<td>r3 = y</td>
</tr>
<tr>
<td>3: r2 = x</td>
<td></td>
</tr>
</tbody>
</table>

\[ x = y = 0 \]
Synchronization: Memory synchronization and fences

Synchronization: Enforces constraint among parallel events.

- done=true;
- while (done) ;
- done = false;
- Value may be present in cache. cache coherence may take care.
- Value may be present in a register - Culprit compiler.
- Value may not be read. How?

<table>
<thead>
<tr>
<th>x = y = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thread 1</td>
</tr>
<tr>
<td>1: r1 = x</td>
</tr>
<tr>
<td>2: y = 1</td>
</tr>
<tr>
<td>3: r2 = x</td>
</tr>
<tr>
<td>Thread 2</td>
</tr>
<tr>
<td>4: x = 1</td>
</tr>
<tr>
<td>r3 = y</td>
</tr>
<tr>
<td>r1 == r2 == r3 == 0. Possible?</td>
</tr>
</tbody>
</table>
A memory fences guarantees that the UEs will see a consistent view of memory.
A memory fences guarantees that the UEs will see a consistent view of memory.

 Writes performed before the fence will be visible to reads performed after the fence.
A memory fence guarantees that the UEs will see a consistent view of memory.

 Writes performed before the fence will be visible to reads performed after the fence.

 Reads performed after the fence will obtain a value written no earlier than the latest write before the fence.
A memory fences guarantees that the UEs will see a consistent view of memory.

- Writes performed before the fence will be visible to reads performed after the fence.
- Reads performed after the fence will obtain a value written no earlier than the latest write before the fence.
- Only for shared memory.
A memory fences guarantees that the UEs will see a consistent view of memory.

 Writes performed before the fence will be visible to reads performed after the fence.

 Reads performed after the fence will obtain a value written no earlier than the latest write before the fence.

 Only for shared memory.

 Explicit management can be error prone. High level: OpenMP flush, shared, Java - volatile. *Read yourself.*
Barrier is a synchronization point at which every member of a collection of UEs must arrive before any member can proceed.

- MPI_Barrier, join, finish, clocks, phasers
- Implemented underneath via passing messages.
Phasers

- Phaser allocation
  - Phaser \( \text{ph} = \text{new Phaser}(\text{mode}) \)
    - Phaser \( \text{ph} \) is allocated with registration mode
    - Mode: SINGLE
      - Mode defines capability
      - There is a lattice ordering of capabilities
    - SIG_WAIT (default)
    - SIGNAL
    - WAIT

- Activity registration
  - async phased (\( \text{ph}_1<\text{mode}_1>, \text{ph}_2<\text{mode}_2>, \ldots \)) \{STMT\}
    - Spawned activity is registered with \( \text{ph}_1 \) in \( \text{mode}_1 \), \( \text{ph}_2 \) in \( \text{mode}_2 \), ...
    - child activity’s capabilities must be subset of parent’s

- Synchronization
  - next:
    - Advance each phaser that activity is registered on to its next phase
    - Semantics depends on registration mode

---

\(^1\) Thanks - Jun Shirako
Power of Phaser - pipeline parallelism

```java
finish {
    phaser [] ph = new phaser[m+1];
    foreach (point [i] : [1:m-1]) phased (ph[i]<SIG>, ph[i-1]<WAIT>)
        for (int j = 1; j < n; j++) {
            a[i][j] = foo(a[i][j], a[i][j-1], a[i-1][j-1]);
            next;
        } // for
    } // foreach
} // finish
```

\[ j \]

\[ i \]

\[ (1,1) \quad (2,1) \quad (3,1) \quad (4,1) \]
\[ (1,2) \]
\[ (1,3) \]
\[ (1,4) \]

\[ A_1 \quad A_2 \quad A_3 \quad A_4 \]

\[ A_1 \]
\[ (i=1, j=1) \quad (i=2, j=1) \quad (i=3, j=1) \quad (i=4, j=1) \]
\[ \text{next} \quad \text{next} \quad \text{next} \quad \text{next} \]
\[ A_2 \]
\[ (i=1, j=2) \quad (i=2, j=2) \quad (i=3, j=2) \quad (i=4, j=2) \]
\[ \text{next} \quad \text{next} \quad \text{next} \quad \text{next} \]
\[ A_3 \]
\[ (i=1, j=3) \quad (i=2, j=3) \quad (i=3, j=3) \quad (i=3, j=3) \]
\[ \text{next} \quad \text{next} \quad \text{next} \quad \text{next} \]
\[ A_4 \]
\[ (i=1, j=4) \quad (i=2, j=4) \quad (i=3, j=4) \quad (i=3, j=4) \]
\[ \text{next} \quad \text{next} \quad \text{next} \quad \text{next} \]

\[ \text{: Loop carried dependence} \]

\[ ^2 \text{Thanks - Jun Shirako} \]
Syncrhonization

- Memory fence
- Barriers
- Mutual exclusion: Java `synchronized`, `omp_set_lock`, `omp_unset_lock`, not required for MPI. Why?
UEs need to exchange information.

- Shared memory - easy. Challenge - synchronize the memory access so that results are correct irrespective of scheduling.
- Distributed memory - not much need for synchronization to protect the resources. → Communication plays a big role.

One to one communication:

- Between all UEs in one event: Collective communication.
Collective communication

When multiple UEs participate in a single communication event, the event is called a collective communication operation. Examples:

- Broadcast: a mechanism to send single message to all UEs.
Collective communication

When multiple UEs participate in a single communication event, the event is called a collective communication operation. Examples:

- **Broadcast**: a mechanism to send single message to all UEs.
- **Barriers**: a synchronization point.
Collective communication

When multiple UEs participate in a single communication event, the event is called a collective communication operation. Examples:

- **Broadcast**: a mechanism to send single message to all UEs.
- **Barriers**: a synchronization point.
- **Reduction**: Take a collection of objects, one from each UE, and "combine" into a single value;
Collective communication

When multiple UEs participate in a single communication event, the event is called a collective communication operation. Examples:

- **Broadcast**: a mechanism to send a single message to all UEs.
- **Barriers**: a synchronization point.
- **Reduction**: Take a collection of objects, one from each UE, and "combine" into a single value;
  - combined value present only on one UE?
When multiple UEs participate in a single communication event, the event is called a collective communication operation. Examples:

- **Broadcast**: a mechanism to send single message to all UEs.
- **Barriers**: a synchronization point.
- **Reduction**: Take a collection of objects, one from each UE, and “combine” into a single value;
  - combined value present only on one UE?
  - combined value present on all UEs?
Tree based reduction

Reduction with 2^n items takes n steps.

What if number of UEs < number of data items?

Only one UE knows the result.

Associative + Commutative or don't care (example?)
Tree based reduction

Reduction with $2^n$ items takes $n$ steps.
Tree based reduction

- Reduction with $2^n$ items takes $n$ steps.
- What if number of UEs $< \text{number of data items}$?
Tree based reduction

- Reduction with $2^n$ items takes $n$ steps.
- What if number of UEs < number of data items?
- Only one UE knows the result.
Tree based reduction

- Reduction with $2^n$ items takes $n$ steps.
- What if number of UEs < number of data items?
- Only one UE knows the result.
- Associative + Commutative or don’t care (example?)
Recursive doubling

Reduction with $2 \times n$ items takes $n$ steps.

What if number of UEs < number of data items?

Only one UE knows the result.
Recursive doubling

- Reduction with $2 \times n$ items takes $n$ steps.
Recursive doubling

- Reduction with $2 \times n$ items takes $n$ steps.
- What if number of UEs < number of data items?
Recursive doubling

- Reduction with $2 \times n$ items takes $n$ steps.
- What if number of UEs < number of data items?
- Only one UE knows the result.
Serial reduction

Reduction with $n$ items takes $n$ steps.

Useful especially if the reduction operator is not associative.

Only one UE knows the result.
Serial reduction

- Reduction with \( n \) items takes \( n \) steps.
Serial reduction

- Reduction with $n$ items takes $n$ steps.
- Useful especially if the reduction operator is not associative.
Serial reduction

- Reduction with $n$ items takes $n$ steps.
- Useful especially if the reduction operator is not associative.
- Only one UE knows the result.
Implementation Mechanisms

- Finding Concurrency
- Algorithm Structure
- Supporting Structures

- Implementation Mechanisms
  - UE Management
  - Synchronization
  - Communication
Part II

Memory Models
Memory Consistency Models

A memory consistency model is a set of rules governing how the memory systems will process memory operations from multiple processors. The order in which memory operations will appear to execute determines what value a read should return. This is a contract between the programmer and the system. It determines what optimizations can be performed for correct programs. Affects ease of programming and performance.
A memory consistency model is a contract between the programmer and the system that determines what optimizations can be performed for correct programs. It affects the ease of programming and performance.

- A memory consistency model is
A memory consistency model is a set of rules governing how the memory systems will process memory operations from multiple processors.
A memory consistency model is a set of rules governing how the memory systems will process memory operations from multiple processors. Order in which memory operations will appear to execute determines what value should a read return.
A memory consistency model is
- a set of rules governing how the memory systems will process memory operations from multiple processors.
  - Order in which memory operations will appear to execute - determines what value should a \textit{read} return?
- a contract between programmer and system.
A memory consistency model is
- a set of rules governing how the memory systems will process memory operations from multiple processors.
  - Order in which memory operations will appear to execute - determines what value should a read return?
- a contract between programmer and system.
- Determines what optimizations can be performed for correct programs.
A memory consistency model is
- a set of rules governing how the memory systems will process memory operations from multiple processors.
  - Order in which memory operations will appear to execute - determines what value should a \textit{read} return?
- a contract between programmer and system.
- Determines what optimizations can be performed for correct programs.

\textbf{Affects:} \textit{Ease of programming, and performance}
Memory value requirement: Memory operations occur in program order: read returns the value of the last write in program order.

- Simple to reason about.
- Compiler optimizations preserve these semantics.
- Independent operations can execute in parallel.
Strict consistency

- Strictest memory model.
- Requires that the ‘read’ should get the value written by the last ‘write’.
Strict consistency

- Strictest memory model.
- Requires that the ‘read’ should get the value written by the last ‘write’.
- Requires a *Global* clock
Strict consistency

- Strictest memory model.
- Requires that the ‘read’ should get the value written by the last ‘write’.
- Requires a *Global* clock \(\equiv\) Halting problem.
Sequential consistency

[Lamport] “A multiprocessor system is sequentially consistent if the result of any execution is the same as if the operations of all processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by the program”
Sequential consistency

Result of an execution appears as if:

- All operations executed in some sequential order.
- Memory operations of each process in program order.
- Nothing specified about caches, write buffers.
Initially Flag1 = Flag2 = 0

P1
Flag1 = 1
if (Flag2 == 0)
   \textit{critical section}

P2
Flag2 = 1
if (Flag1 == 0)
   \textit{critical section}

Execution:

P1
\begin{itemize}
\item \textit{(Operation, Location, Value)}
\item Write, Flag1, 1
\item Read, Flag2, 0
\end{itemize}

P2
\begin{itemize}
\item \textit{(Operation, Location, Value)}
\item Write, Flag2, 1
\item Read, Flag1, ___
\end{itemize}
Initially Flag1 = Flag2 = 0

P1
Flag1 = 1
if (Flag2 == 0)
    \textit{critical section}

P2
Flag2 = 1
if (Flag1 == 0)
    \textit{critical section}

Execution:

P1
(\textit{Operation, Location, Value})
Write, Flag1, 1
Read, Flag2, 0

P2
(\textit{Operation, Location, Value})
Write, Flag2, 1
Read, Flag1, \textcolor{red}{X}
Initially Flag1 = Flag2 = 0

P1
Flag1 = 1
if (Flag2 == 0)
    critical section

P2
Flag2 = 1
if (Flag1 == 0)
    critical section

Execution:
P1
(Operation, Location, Value)
Write, Flag1, 1

Read, Flag2, 0

P2
(Operation, Location, Value)
Write, Flag2, 1

Problematic situation
- Write buffers with read bypassing.
Understanding Program Order. Dekker’s Algorithm

Initially Flag1 = Flag2 = 0

P1
Flag1 = 1
if (Flag2 == 0)
    critical section

P2
Flag2 = 1
if (Flag1 == 0)
    critical section

Execution:

P1
(Operation, Location, Value)
Write, Flag1, 1
Read, Flag2, 0

P2
(Operation, Location, Value)
Write, Flag2, 1
Read, Flag1,

Problematic situation

- Write buffers with read bypassing.
- Overlap or reorder writes/reads by compiler / hardware.
Understanding Program Order. Dekker’s Algorithm

Initially Flag1 = Flag2 = 0

P1
Flag1 = 1
if (Flag2 == 0)  
    critical section

P2
Flag2 = 1
if (Flag1 == 0)  
    critical section

Execution:

P1
(Operation, Location, Value)
Write, Flag1, 1
Read, Flag2, 0

P2
(Operation, Location, Value)
Write, Flag2, 1
Read, Flag1, 0

Problematic situation

- Write buffers with read bypassing.
- Overlap or reorder writes/reads by compiler / hardware.
- Values in registers.
Initially $A = Flag = 0$

P1
A = 23;
Flag = 1;

P2
while (Flag != 1) {};
... = A;

P1
Write, A, 23
Write, Flag, 1

P2
Read, Flag, 0
Read, Flag, 1
Read, A, ___
Initially $A = \text{Flag} = 0$

P1
A = 23;
Flag = 1;

P2
while (Flag != 1) {};
... = A;

P1
Write, A, 23
Write, Flag, 1

P2
Read, Flag, 0
Read, Flag, 1
Read, A, 0
Understanding Program Order. Ex 2

Initially $A = \text{Flag} = 0$

$P1$
$A = 23;$
$\text{Flag} = 1;$

$P2$
while $(\text{Flag} \neq 1)$ {
...
$= A;$
}

$P1$
Write, $A$, 23
Write, $\text{Flag}$, 1

$P2$
Read, $\text{Flag}$, 0
Read, $\text{Flag}$, 1
Read, $A$, 0

Problematic situation

- Overlap or reorder writes/reads by compiler / hardware.
Initially $A = B = C = 0$

P1    P2    P3    P4
A = 1;  A = 2;  while (B != 1) ;  while (B != 1) ;
B = 1;  C = 1;  while (C != 1) ;  while (C != 1) ;
    tmp1 = A;  tmp2 = A;

Q: What are the possible values of tmp1 and tmp2?

Cache coherence protocol must serialize writes to same location. Writes to same location should be seen in same order by all.
Write Atomicity

Initially $A = B = C = 0$

P1 | P2 | P3 | P4
---|---|---|---
$A = 1$; $A = 2$; while ($B \neq 1$); while ($B \neq 1$);  
$B = 1$; $C = 1$; while ($C \neq 1$); while ($C \neq 1$);
  tmp1 = $A$;  
  tmp2 = $A$;

Q: What are the possible values of tmp1 and tmp2?
Q: Can tmp1 = 1 and tmp2 = 2 be possible? How?
Write Atomicity

Initially $A = B = C = 0$

P1    P2    P3    P4
A = 1; A = 2; while (B != 1); while (B != 1);
B = 1; C = 1; while (C != 1); while (C != 1);

tmp1 = A; tmp2 = A;

Q: What are the possible values of tmp1 and tmp2?
Q: Can tmp1 = 1 and tmp2 = 2 be possible? How?

- Cache coherence protocol must serialize writes to same location.
- Writes to same location should be seen in same order by all.
Initially $A = B = 0$

P1
$A = 1$

P2
while ($A != 1$) ;

$B = 1$

P3
tmp = $A$

P1
Write, A, 1

P2
Read, A, 1
Write, B, 1

P3
Read, B, 1
Read, A, ✗
Initially $A = B = 0$

P1

A = 1

P2

while (A != 1) ;
B = 1;

P3

tmp = A

P1

Write, A, 1

P2

Read, A, 1
Write, B, 1

P3

Read, B, 1

Read, A, ✗

- if 'read' returns a new value before all copies see it.
Initially $A = B = 0$

P1

$A = 1$

P2

while ($A != 1$); while ($B != 1$);

B = 1;

tmp = A

P3

\[ \text{if ‘read’ returns a new value before all copies see it.} \]

\[ \text{Read others’-write early optimization is unsafe.} \]
Implementations of this model must satisfy the following:

- **Program Order Requirement**: The operations of the same processor must be executed in program order.

- **Write Atomicity**: All writes appear to be instantaneous (no buffer). All processors must see all write operations in the same order (cache coherence).

Easier to implement in architectures with no cache, no write buffers, blocking reads.
Implementations of this model must satisfy the following:

- **Program Order Requirement**: The operations of the same processor must be executed in program order.

- **Write Atomicity**: All writes appear to be instantaneous (no buffer).
Implementations of this model must satisfy the following:

- **Program Order Requirement**: The operations of same processor must be executed in program order.
- **Write Atomicity**: All writes appear to be instantaneous (no buffer).
- All processors must see all write operations in the same order (cache coherence).
Implementations of this model must satisfy the following:

- **Program Order Requirement**: The operations of same processor must be executed in program order.
- **Write Atomicity**: All writes appear to be instantaneous (no buffer).
- All processors must see all write operations in the same order (cache coherence).
- Easier to implement in architectures with no cache, no write buffers, blocking reads...
Sequential Consistency - issues

- Sequential Consistency constraints
  - write → read
  - write → write
  - read → read
  - read → write

Implications (not allowed)
- Read others' write early.
- Read own write early.
- Unserialized writes to the same location.

Simple model to reason about given parallel programs.
Makes it very hard to modify a parallel program (automatic and manual)
Processor reordering for performance - write buffers, overlapped writes, non-blocking reads
Compiler transformations - scalar replacement, register allocation, instruction scheduling.
Programmer reordering code for aesthetics/SE requirements.
Sequential Consistency - issues

- Sequential Consistency constraints
  - write $\rightarrow$ read
  - write $\rightarrow$ write
  - read $\rightarrow$ read
  - read $\rightarrow$ write

Implications (not allowed)
- Read others’ write early.
- Read own write early.
- Unserialized writes to the same location.
Sequential Consistency - issues

- Sequential Consistency constraints
  - write → read
  - write → write
  - read → read
  - read → write

- Implications (not allowed)
  - Read others’ write early.
  - Read own write early.
  - Unserialized writes to the same location.

- Simple model to reason about given parallel programs.
Sequential Consistency - issues

- Sequential Consistency constraints
  - write $\rightarrow$ read
  - write $\rightarrow$ write
  - read $\rightarrow$ read
  - read $\rightarrow$ write

Implications (not allowed)
- Read others’ write early.
- Read own write early.
- Unserialized writes to the same location.

- Simple model to reason about given parallel programs.
- Makes it very hard to modify a parallel program (automatic and manual)
  - Processor reordering for performance - write buffers, overlapped writes, non-blocking reads
Sequential Consistency - issues

- Sequential Consistency constraints
  - write → read
  - write → write
  - read → read
  - read → write

Implications (not allowed)
  - Read others’ write early.
  - Read own write early.
  - Unserialized writes to the same location.

- Simple model to reason about given parallel programs.
- Makes it very hard to modify a parallel program (automatic and manual)
  - Processor reordering for performance - write buffers, overlapped writes, non-blocking reads
  - Compiler transformations - scalar replacement, register allocation, instruction scheduling.
Sequential Consistency - issues

- Sequential Consistency constraints
  - write → read
  - write → write
  - read → read
  - read → write

  Implications (not allowed)
  - Read others’ write early.
  - Read own write early.
  - Unserialized writes to the same location.

- Simple model to reason about given parallel programs.
- Makes it very hard to modify a parallel program (automatic and manual)
  - Processor reordering for performance - write buffers, overlapped writes, non-blocking reads
  - Compiler transformations - scalar replacement, register allocation, instruction scheduling.
  - Programmer reordering code for aesthetics/SE requirements.
Sequential consistency - too strict

- Many architectures do not give SC.
- Compiler optimizations on SC are limited.
- Software engineering issues.

- Give up!
- Use weaker models - relax the program order requirement and write atomicity requirement.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by the same processor or access the same memory location - are seen by every node in the same order.

Causal order is transitive. Memory operations that are causally related must have a total order and program order for the ones issued by the same processor. Hence such memory operations must be seen in the same order by all processors. Here, write atomicity has been slightly weakened, weaker than sequential consistency, which requires that all nodes see all writes in the same order.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by same processor or access same memory location - are seen by every node in the same order.
- Causal order is transitive.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by same processor or access same memory location - are seen by every node in the same order.
- Causal order is transitive.
  - memory operations that are causally related must have a total order and
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by the same processor or access the same memory location are seen by every node in the same order.
- Causal order is transitive.
  - Memory operations that are causally related must have a total order and
  - Program order for the ones issued by the same processor.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by same processor or access same memory location - are seen by every node in the same order.
- Causal order is transitive.
  - memory operations that are causally related must have a total order and
  - program order for the ones issued by same processor.
- Hence such memory operations must be seen in same order by all processors.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by same processor or access same memory location - are seen by every node in the same order.
- Causal order is transitive.
  - memory operations that are causally related must have a total order and
  - program order for the ones issued by same processor.
- Hence such memory operations must be seen in same order by all processors.
- Here, write atomicity has been slightly weakened.
Causal Consistency

- Slightly weaker than Sequential Consistency Model.
- Causally related memory operations: issued by same processor or access same memory location - are seen by every node in the same order.
- Causal order is transitive.
  - memory operations that are causally related must have a total order and
  - program order for the ones issued by same processor.
- Hence such memory operations must be seen in same order by all processors.
- Here, write atomicity has been slightly weakened.
- weaker than sequential consistency, which requires that all nodes see all writes in the same order.
PRAM consistency

- All processes see memory writes from one process in the order they were issued from the process.
PRAM consistency

- All processes see memory writes from one process in the order they were issued from the process.
- Writes from different processes may be seen in a different order on different processes.
PRAM consistency

- All processes see memory writes from one process in the order they were issued from the process.
- Writes from different processes may be seen in a different order on different processes.
- No guarantees about the order in which different processes see writes, except that two or more writes from a single source must arrive in order, as though they were in a pipeline.

\[
P_1: W(x)1 \\
P_2: R(x)1 W(x)2 \\
P_3: \\
P_4: R(x)1 R(x)2 \\
\text{Time ----> } R(x)2 R(x)1
\]
PRAM consistency

- All processes see memory writes from one process in the order they were issued from the process.
- Writes from different processes may be seen in a different order on different processes.
- No guarantees about the order in which different processes see writes, except that two or more writes from a single source must arrive in order, as though they were in a pipeline.

\[
\begin{align*}
P1: & \quad W(x)1 \\
P2: & \quad R(x)1 W(x)2 \\
P3: & \quad R(x)1 R(x)2 \\
P4: & \quad R(x)2 R(x)1 \\
Time: & \quad ----->
\end{align*}
\]

- PRAM \(\leq\) Causal \(\leq\) SC \(\leq\) Strict
PRAM consistency

- All processes see memory writes from one process in the order they were issued from the process.
- Writes from different processes may be seen in a different order on different processes.
- no guarantees about the order in which different processes see writes, except that two or more writes from a single source must arrive in order, as though they were in a pipeline.

PRAM \leq \text{Causal} \leq \text{SC} \leq \text{Strict}

(Also known as, FIFO consistency, or Processor consistency)
Weak Ordering

- Divide memory operations into data operations and synchronization operations

Synchronization operations act like a fence.
All data operations before synch in program order must complete before synch is executed.
All data operations after synch in program order must wait for synch to complete.
Synchronizations are performed in program order.
All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
All other accesses may be seen in different order on different processes.
Illusion of write atomicy has to be maintained.

Hardware implementation of fence: processor has counter that is incremented when data op is issued, and decremented when data op is completed.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
- All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
- All other accesses may be seen in different order on different processes.
- Illusion of write atomicy has to be maintained.
- Hardware implementation of fence: processor has counter that is incremented when data op is issued, and decremented when data op is completed.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
- Synchronizations are performed in program order.
Weak Ordering

- Divide memory operations into data operations and synchronization operations.
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
- Synchronizations are performed in program order.
- All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
- Synchronizations are performed in program order.
- All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
- All other accesses may be seen in different order on different processes
Weak Ordering

- Divide memory operations into data operations and synchronization operations.
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
- Synchronizations are performed in program order.
- All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
- All other accesses may be seen in different order on different processes.
- Illusion of write atomicy has to be maintained.
Weak Ordering

- Divide memory operations into data operations and synchronization operations
- Synchronization operations act like a fence.
  - All data operations before synch in program order must complete before synch is executed.
  - All data operations after synch in program order must wait for synch to complete.
- Synchronizations are performed in program order.
- All accesses to synchronization variables are seen by all processes (or nodes, processors) in the same order (sequentially) - these are synchronization operations. Accesses to critical sections are seen sequentially.
- All other accesses may be seen in different order on different processes
- Illusion of write atomicity has to be maintained.
- Hardware implementation of fence: processor has counter that is incremented when data op is issued, and decremented when data op is completed.
Weak Ordering

Example 1:

\[
\begin{align*}
\text{P1} & \quad W(x)_1 \quad W(x)_2 \quad \text{Sync} \\
\text{P2} & \quad \text{Sync} \\
\text{P3} & \quad R(x)_2 \quad R(x)_1 \quad \text{Sync}
\end{align*}
\]
Weak Ordering

Example 1:

- P1: \( W(x)1 \) \( W(x)2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- P3: \( R(x)2 \) \( R(x)1 \) \( \text{Sync} \)

Example 2:

- P1: \( W(x)1 \) \( W(x)2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- R(x)1

The programmer has to manage synchronization explicitly.

Weak \( \leq \) PRAM \( \leq \) Causal \( \leq \) SC \( \leq \) Strict
Weak Ordering

Example 1:

- P1: \( W(x)_1 \) \( W(x)_2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- P3: \( \text{Sync} \)

Example 2:

- P1: \( W(x)_1 \) \( W(x)_2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- R(x): \( \text{Sync} \)
- R(x)_2 \( \text{Sync} \)
Weak Ordering

Example 1:
- P1: \( W(x)_1 \) \( W(x)_2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- P3: \( R(x)_2 \) \( R(x)_1 \) \( \text{Sync} \)

Example 2:
- P1: \( W(x)_1 \) \( W(x)_2 \) \( \text{Sync} \)
- P2: \( \text{Sync} \)
- P3: \( \text{Sync} \) \( R(x)_1 \)
Weak Ordering

Example 1:

P1 \( W(x)1 \ W(x)2 \ Sync \)
P2 \( R(x)1 \ R(x)2 \ Sync \)
P3 \( R(x)2 \ R(x)1 \ Sync \)

Example 2:

P1 \( W(x)1 \ W(x)2 \ Sync \)
P2 \( Sync \)
R(x)1

The programmer has to manage synchronization explicitly.
Weak Ordering

Example 1:

\begin{align*}
\text{P1} & \quad \text{W(x)1} \quad \text{W(x)2} \quad \text{Sync} \\
\text{P2} & \\
\text{P3} & \quad \text{R(x)1} \quad \text{R(x)2} \quad \text{Sync} \\
\end{align*}

Example 2:

\begin{align*}
\text{P1} & \quad \text{W(x)1} \quad \text{W(x)2} \quad \text{Sync} \\
\text{P2} & \quad \text{Sync} \quad \text{R(x)1} \\
\end{align*}

The programmer has to manage synchronization explicitly.

Weak $\leq$ PRAM $\leq$ Causal $\leq$ SC $\leq$ Strict
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release: Must be executed only when all memory operations statements are complete. But accesses after 'release' in program order do not have to wait for release (unless protected by another acquire).
- "acquire" = that writes on other processors to protected variables will be known.
- "release" = that writes to protected variables are exported and will be seen by other machines when they do a lock (lazy release consistency) or immediately (eager release consistency).
- Total order among all synchronization instructions must be maintained.
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release:
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release:
  - Release must be executed only when all memory operations statements are complete.

**Lazy release consistency**
- Do “acquire” = that writes on other processors to protected variables will be known.
- Do “release” = that writes to protected variables are exported and will be seen by other machines when they do a lock.

**Total order among all synchronization instructions must be maintained.**
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release:
  - Release must be executed only when all memory operations statements are complete.
  - But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release:
  - Release must be executed only when all memory operations statements are complete.
  - But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).
- do “acquire” = that writes on other processors to protected variables will be known
Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).

Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).

Release:
- Release must be executed only when all memory operations statements are complete.
- But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).

do “acquire” = that writes on other processors to protected variables will be known

do “release” = that writes to protected variables are exported
Release Consistency

- Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release:
  - Release must be executed only when all memory operations statements are complete.
  - But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).
- do “acquire” = that writes on other processors to protected variables will be known
- do “release” = that writes to protected variables are exported and will be seen by other machines when they do a lock (lazy release consistency) or immediately (eager release consistency)
Synchronization instructions divided: Acquire (such as lock) and Release (such as unlock).

Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).

Release:
- Release must be executed only when all memory operations statements are complete.
- But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).

Do “acquire” = that writes on other processors to protected variables will be known

Do “release” = that writes to protected variables are exported and will be seen by other machines when they do a lock (lazy release consistency) or immediately (eager release consistency)

Total order among all synchronization instructions must be maintained.
Release Consistency - example

P1: L W(x)1 W(x)2 U

Example: P2: L R(x)2 U
P3: R(x)1

RC ≤ Weak ≤ PRAM ≤ Causal ≤ SC ≤ Strict
Delta and Eventual consistency models

- **Delta consistency**: The write operations will propagate through the shared memory system and all the replicas will be consistent after a fixed time period $\delta$.

- **Eventual Consistency Model**: The writes propagate eventually (we cannot have a fixed bound on the delay).
Delta and Eventual consistency models

- **Delta consistency**: The write operations will propagate through the shared memory system and all the replicas will be consistent after a fixed time period $\delta$.
  - if an object is modified, during the short period of time following its modification, the read may not be consistent.
**Delta consistency**: The write operations will propagate through the shared memory system and all the replicas will be consistent after a fixed time period $\delta$.

- if an object is modified, during the short period of time following its modification, the read may not be consistent.
- after a fixed time period, the modification is propagated and the read will be consistent.
Delta and Eventual consistency models

- **Delta consistency**: The write operations will propagate through the shared memory system and all the replicas will be consistent after a fixed time period $\delta$.
  - if an object is modified, during the short period of time following its modification, the read may not be consistent.
  - after a fixed time period, the modification is propagated and the read will be consistent.

- **Eventual Consistency Model**: The writes propagates eventually (we cannot have a fixed bound on the delay)
Problem with relaxed models is that most of them are based on the performance optimization that can be performed. How to reason about programs for systems with relaxed memory models. How to use the safety nets minimally, to get the desired semantics from program. Even Sequential Consistency is not simple enough. We need models which is simple for the programmer, but provides enough information about program to apply optimization and get efficiency.
Problem with relaxed models is that most of them are based on the performance optimization that can be performed. However, from a programmer’s perspective, it is not clear how to use these effectively.
Problem with relaxed models is that most of them are based on the performance optimization that can be performed.

However, from a programmer’s perspective, it is not clear how to use these effectively.

- How to reason about programs for systems with relaxed memory models
Programmer centric models

- Problem with relaxed models is that most of them are based on the performance optimization that can be performed.
- However, from a programmer’s perspective, it is not clear how to use these effectively.
  - How to reason about programs for systems with relaxed memory models
  - How to use the safety nets minimally, to get the desired semantics from program
Programmer centric models

- Problem with relaxed models is that most of them are based on the performance optimization that can be performed.
- However, from a programmer’s perspective, it is not clear how to use these effectively.
  - How to reason about programs for systems with relaxed memory models
  - How to use the safety nets minimally, to get the desired semantics from program
- Even Sequential Consistency is not simple enough.
Programmer centric models

- Problem with relaxed models is that most of them are based on the performance optimization that can be performed.
- However, from a programmer’s perspective, it is not clear how to use these effectively.
  - How to reason about programs for systems with relaxed memory models
  - How to use the safety nets minimally, to get the desired semantics from program
- Even Sequential Consistency is not simple enough.
- We need models which is simple for the programmer, but provides enough information about program to apply optimization and get efficiency.
Programmers understand their code:

- Different operations have different semantics
  
<table>
<thead>
<tr>
<th>P1</th>
<th>P2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = 23;</td>
<td>while (Flag != 1) ;</td>
</tr>
<tr>
<td>B = 37;</td>
<td>... = B;</td>
</tr>
<tr>
<td>Flag = 1;</td>
<td>... = A;</td>
</tr>
</tbody>
</table>

- Flag = Synchronization; A, B = Data
- Can reorder data operations
- Distinguish data and synchronization
• **Data-Race-Free-0 Program**
  — All accesses distinguished as either *synchronization* or *data*
  — All *races* distinguished as *synchronization* (in any SC execution)

• **Data-Race-Free-0 Model**
  — Guarantees SC to data-race-free-0 programs
  — *(For others, reads return value of some write to the location)*
• Information required:
  — *This operation never races* (in any SC execution)

1. Write program assuming SC
2. For every memory operation specified in the program do:

   Distinguish as *data*

   - yes
     - Never races?
     - no
     - Distinguish as *synchronization*

   - don’t know or don’t care
Problems with data race free model

- It does not define any semantics for programs with data races.
- A concern for safe languages like Java, which provide safety for any program and cannot let the behavior of a program to be ambiguous.
- Either define safe semantics for such programs or identify them and prevent their execution.
- Define higher abstractions for programmers which are inherently data race free.
- Expensive for hardware to implement.
Goals of Memory model

- Programmability? - Lost intuitive interface of SC
- Portability? - Many different models
- Performance? - Can we do better?

Future:
- Parallel programs today are inherently non deterministic
- We need deterministic outcomes from our parallel programs.
- Deterministic Outcomes from Inherent non determinism. Possible?
Patterns for Parallel Programming: Sandors, Massingills.
multicoreinfo.com
Wikipedia
fixstars.com
Jernej Barbic slides.
Loop Chunking in the presence of synchronization.
Vivek Sarkar’s slides.
Sarita Adve’s slides.
Nimit’s Singhania’s presentation.
Java Memory Model JSR-133: “Java Memory Model and Thread Specification Revision”
Questions?
Answers are not guaranteed!

It’s a shame the world is so full of conflict.
On the other hand, I’m a lawyer.

Reseacher!