A Wide Power-Supply Range (0.5V-to-1.3V) Wide Tuning Range (500 MHz-to-8 GHz) All-Static CMOS ADPLL in 65nm SOI

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PLL for Microprocessors and ASICs

- Low period jitter needed to increase usable cycle time
- Lots of programmability needed for ASIC applications
- ADPLL performance should track other digital circuits over manufacturing corners
All Digital PLL (ADPLL) Architecture

- BB (Bandpass Filter)
- PFD (Phase-Frequency Detector)
- Digital PID Filter
- \( \Sigma \Delta \)
- Divide-by-N Clock
- Divide-by-M Gate
- Clock Divider
- SCLK (Serial Clock Input)
- Data In
- Data Out
- Vdda
- DCO (Direct Current Oscillator)
- DCC Buffer
- Serial Interface Control and Registers
- Ref Clock
- Early/Late
- MSB
- LSB
- Clock Out
Self-timed Bang-bang PFD

Asynchronous Reset

Ref Leads (Late)

Div Leads (Early)

C-element
Mutual-exclusion Element (Mutex)

Mutex detects which of A or B makes a high-to-low transition first. It is reset by A and B going high.

These nodes may go metastable.

$A_{First}$ and $B_{First}$ are not resolved until $A_u$ and $B_u$ differ by at least $V_{th}$.
PID Loop Filter Architecture

5-bit arithmetic combines with the DCO control to implement 14-bit arithmetic.
3rd Order MASH ΣΔ

Fractional Frequency From Loop Filter

To Dithered Control
DCO Inverter Array and Control

From Sigma Delta / Loop Filter

Dither Control

Row Override

Row Control

From Loop Filter

Shift Control

Inverter Array

Column Control

Phase0

Phase1

Phase2

271 Inverters per phase
DCO Control

Loop Filter
Underflow/Overflow

Shift by -1, 0, 1

csel0
csel1
csel2

Column Underflow / Overflow

'1'

Shift by -1, 0, 1

rsel0
rsel1
rsel2

Row Even/Odd/First/Last

Column Control

Row Control
DCO Array

Some inverters are turned off

Some inverters are turned on

Output frequency a function of “filling factor”: fraction of tri-state inverters turned on

Phase 0
Phase 1
Phase 2
Single Tri-state Inverter with Control

Also performs conversion from VDD to VDDA

Phase (i mod 3)

Phase ((i+1) mod 3)

csel i (j even)
Not csel i (j odd)
Design for Manufacturing Test

- All digital logic is connected to a scan chain, and is LSSD testable (Level Sensitive Scan Design)
- The only “analog” component, the ring oscillator, can be tested this way as well
- Checking for locking range can be executed digitally
ADPLL Floorplan, 65 nm SOI
## Design Summary

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCO (Digitally Controlled Oscillator)</td>
<td>Three stage ring oscillator. Tri-state inverters switched on-off to change gm of the ring stages. 800 frequency steps</td>
</tr>
</tbody>
</table>
| Loop filter                  | Digital PID filter running at divided frequency. 1 MHz to 20 MHz programmable loop bandwidth  
Third order MASH Sigma Delta |
| PFD                          | Self-timed, bang-bang PFD                                                                                                                                                                                  |
| Area                         | 200 μm × 150 μm, generously floor-planned layout                                                                                                                                                           |

All static standard cell CMOS in 65nm SOI, 2 versions (HVT, RVT FETs). Custom design for tri-state inverter and metastability filter.
VHDL Simulations

Frequency / Phase acquisition
Pink -> reference cycle time
White -> output clock cycle time

Zero-crossing data is passed to Matlab for spectral processing
Simulated Phase Noise Plot

Phase Noise (dEc/Hz)

-150 -140 -130 -120 -110 -100 -90 -80

Frequency (MHz)

$10^{-2}$ $10^{-1}$ $10^{0}$ $10^{1}$ $10^{2}$ $10^{3}$

No Sigma Delta

First and second order Sigma Delta

SD2
SD1
SD0
Simulated Phase Noise Plot

- No Sigma Delta
- First and second order Sigma Delta
Closed Loop Phase Noise, 4 GHz, 1.2V, 100°C

<table>
<thead>
<tr>
<th>Freq Offset</th>
<th>2nd Order ΣΔ</th>
<th>1st Order ΣΔ</th>
<th>0th Order ΣΔ</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kHz</td>
<td>-97.10 dBc/Hz</td>
<td>-98.59 dBc/Hz</td>
<td>-98.12 dBc/Hz</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-102.84 dBc/Hz</td>
<td>-100.94 dBc/Hz</td>
<td>-100.62 dBc/Hz</td>
</tr>
<tr>
<td>1 MHz</td>
<td>-111.22 dBc/Hz</td>
<td>-107.36 dBc/Hz</td>
<td>-101.69 dBc/Hz</td>
</tr>
<tr>
<td>10 MHz</td>
<td>-112.11 dBc/Hz</td>
<td>-109.94 dBc/Hz</td>
<td>-98.90 dBc/Hz</td>
</tr>
<tr>
<td>100 MHz</td>
<td>-118.68 dBc/Hz</td>
<td>-114.70 dBc/Hz</td>
<td>-118.95 dBc/Hz</td>
</tr>
<tr>
<td>1 GHz</td>
<td>-130.99 dBc/Hz</td>
<td>-126.61 dBc/Hz</td>
<td>-125.39 dBc/Hz</td>
</tr>
</tbody>
</table>
Period Jitter, 4GHz Output, 0.5 GHz Ref.,
1.2V Supply, 100ºC, 2\textsuperscript{nd} Order $\Sigma\Delta$

<table>
<thead>
<tr>
<th>Mean T\text{cycle}</th>
<th>250 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min T\text{cycle}</td>
<td>246 ps</td>
</tr>
<tr>
<td>Max T\text{cycle}</td>
<td>254 ps</td>
</tr>
<tr>
<td>Std Dev</td>
<td>0.7 ps</td>
</tr>
</tbody>
</table>

In general, $T_1 \neq T_2 \neq \ldots$ Figure is histogram of measured $T_i$'s
**Period Jitter, 1GHz Output, 125 MHz Reference, 0.5V Supply, 100°C, No ΣΔ**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean Tcycle</td>
<td>1000 ps</td>
</tr>
<tr>
<td>Min Tcycle</td>
<td>987 ps</td>
</tr>
<tr>
<td>Max Tcycle</td>
<td>1012 ps</td>
</tr>
<tr>
<td>Std Dev</td>
<td>3.0 ps</td>
</tr>
</tbody>
</table>

Power dissipation: **1.6 mW**
N-Cycle Jitter Accumulation, 1.2V, 100ºC, 4GHz, 2\textsuperscript{nd} Order $\Sigma\Delta$
## Test Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locking range</td>
<td>400 MHz to 8 GHz measured</td>
</tr>
<tr>
<td>Power Supply range</td>
<td>0.5 V -&gt; phase lock up to 1 GHz&lt;br&gt;1.3 V -&gt; phase lock up to 8 GHz (RVT)</td>
</tr>
<tr>
<td>Power</td>
<td>1.6 mW / GHz @ 0.5V&lt;br&gt;8 mW / GHz @ 1.2V</td>
</tr>
<tr>
<td>Jitter (RMS)</td>
<td>Period: 0.7 ps&lt;br&gt;Long term: 5 ps&lt;br&gt;Cycle to cycle: 1.1 ps</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-110 dBC/Hz @ 10 MHz, 500 MHz reference, 4 GHz output, 2nd order ΣΔ</td>
</tr>
</tbody>
</table>
Conclusion

- We designed, simulated and tested an ADPLL in 65 nm SOI
- The ADPLL is ideally suited for µP and ASIC applications in advanced CMOS technology
- All static CMOS implementation allows this circuit to work over a wide voltage range (0.5V to 1.3V)
  - Useful for very low power circuits (1.6 mW @ 1 GHz)
  - Allows for VDD regulation (e.g. from 1.2V down to 0.6V) while still maintaining ASIC level performance
- Digital design = Scalable, testable, predictable