A Modular All Digital PLL Architecture Enabling Both 1-to-2 GHz and 24-to 32-GHz Operation in 65nm CMOS

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Outline

• Introduction
• DPLL architecture and digital design details
• DCO designs
• Measurement results
• Conclusion
Introduction/Motivation

• Modular DPLL architecture demonstrated
  – Realization in 2 GHz ring-based and 6 GHz, 11 GHz, and 32 GHz LC-DCO-based designs
  – Core loop elements common to all

• Custom elements per design restricted to
  – Fractional-N capability added to ring design
  – Extra dividers added to LC-DCO designs to bring feedback clock within usable frequency range
• Common core digital components used in multiple designs
Loop Filter

P = Proportional constant
I = Integral constant

Realized Transfer Functions

integral: \( 1 \times \frac{1}{1 - z^{-1}} \)
proportional: \( (1 - z^{-1}) \times \frac{1}{1 - z^{-1}} \)

8-bit arithmetic realized using Kogge-Stone adder

Merging proportional, integral paths simplifies DPLL logic
8-bit Parallel (Kogge-Stone) Adder

Universal block, used in:
- Loop Filter Integrator
- Feedback Divider
- $\Delta\Sigma$ Accumulators
Divider $\Delta\Sigma M$ vs DCO $\Delta\Sigma M$

- Requires explicit 8-bit adders
- Requires signed arithmetic
- Pipelining requires careful latency matching for proper noise shaping

- Uses DCO as an adder
- Generates DC offset (invisible due to loop action)
- Dithering outputs are applied in parallel with matched delays

\[ N + FN + (z^{-1} - 1) e_1 \quad N + FN + (z^{-1} - 1)^2 e_2 \]
• \textbf{phold} is a masking signal

• \textbf{divided clkg} is compared with \textbf{reference} in PFD

• \textbf{const} can be updated between \textbf{phold} rising edges

*6/11/32 GHz LC-VCO cases
Modular DPLL Architecture: Annotated

BB-PFD → LF → ΔΣM

early/late

coarse

inc/dec

dither

DCO with row/col controls

output

phold

clkg

1/N

1/M

1/16 or 1/4

LC-DCO version

ring-DCO version

output

clkg

phold
5-Stage Ring DCO

- Target frequency range: 1 to 2 GHz
- Target $K_{DCO} < 10$ MHz / inverter
32 GHz LC DCO Topology

Circled elements differ between 32 and 6/11 GHz VCOs [as do L, C values]

Varactor: NFET

dither <1:3>, inc/dec

inc/dec

shift control

row/column logic

coarse <1:4>

cap_hi <1:24>

VDDA

output

output_b

IREF

to 1/16 divider

<1:4>

<1:24>

<1:5>

CML
6, 11 GHz LC DCO Topology

Circled elements differ between 32 and 6/11 GHz VCOs [as do L, C values]

Varactor: accumulation-mode
Ring DCO: Open Loop Tuning Curves

DCO Main Array Fill Factor*

- $K_{DCO} = 2.6$ MHz/inverter at $0.8V$, $100^\circ C$
- $K_{DCO} = 6.1$ MHz/inverter at $1.2V$, $25^\circ C$

*Array Fill Factor = On-state inverters / Total number of inverters
Ring-DPLL: Period Jitter Histogram

Average period: 485.44 ps (2.06 GHz, N = 160)
Jitter: 1.0 ps rms, 16.6 ps peak-to-peak (3.8 million cycles)
Fractional-N Period Jitter Histograms

Reference clock: 25.75 MHz
VDDA=VDD=1.1V, 15mA, 25°C

- N=80: 1.1 ps rms, 16.3 ps pk-to-pk
- N=79.996, 1st order ∆ΣM: 1.2 ps rms, 21.7 ps pk-to-pk
- N=79.996, 2nd order ∆ΣM: 1.5 ps rms, 25.8 ps pk-to-pk

Measured period jitter at 2.06 GHz (1 million cycles)
- N=80: 1.1 ps rms, 16.3 ps pk-to-pk
- N=79.996, 1st order ∆ΣM: 1.2 ps rms, 21.7 ps pk-to-pk
- N=79.996, 2nd order ∆ΣM: 1.5 ps rms, 25.8 ps pk-to-pk
Ring-DPLL Dynamics

N = 97

N = 103

N jumps from 103 to 97

15 MHz reference
I = 2^-8

Frequency: 1.5 GHz center, 110 MHz span
Ring-DPLL Dynamics II

Frequency: 1.5 GHz center, 110 MHz span

N = 97

N = 103

N jumps from 103 to 97

15 MHz reference

I = 2^-6

increase in integration constant reduces relock time
Ring-DPLL Dynamics III

One coarse row is switched off

DPLL relocks to the original frequency by populating an extra row in the main array

Frequency: 2.0 GHz center

110 MHz span

Time, 1.8 ms span
Ring-DPLL Dynamics IV

Same experiment repeated at lower center frequency

One coarse row is switched off

Frequency: 1.9 GHz center
Frequency: 2.0 GHz center

Time, 1.8 ms span

110 MHz span
110 MHz span
Ring-DPLL Dynamics V

Frequency: 1.5 GHz center, 110 MHz span

Time, 2 ms span

One coarse row is switched off and N jumps from 103 to 97

N = 103

15 MHz reference
I = 2^-8

N = 97
32 GHz LC-DCO Tuning Curves

Frequency [GHz] vs. DCO Main Array Fill Factor

- 25°C
- 85°C

K_{\text{DCO}} = 76 MHz per varactor

LC-DCO, 1.5V
Spectrum of 32 GHz Output

Span: 200MHz. Resolution bandwidth: 10kHz.
LC-DPLL Phase Noise Plot at 32 GHz

- measured at VDDA=1.5V (36mA), VDD=1.3V (12.2mA), 25°C, 2 GHz reference
6 and 11 GHz DCO Tuning Curves

1.2V, 100°C

K_{DCO} = 9.5 MHz

1.3V, 25°C

K_{DCO} = 15.6 MHz

Frequency [GHz]

DCO Main Array Fill Factor
6 and 11 GHz DPLL Phase Noise

4.8 GHz, 1.2V, 25°C

10 GHz, 1.3V, 25°C
32 GHz LC-DPLL Die Photograph
# DPLL Performance Summary

<table>
<thead>
<tr>
<th>CMOS Technology</th>
<th>3-stage ring DPLL(^1)</th>
<th>5-stage ring DPLL</th>
<th>LC-tank DPLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>200 µm X 150 µm</td>
<td>180 µm X 270 µm</td>
<td>240 µm X 350 µm</td>
</tr>
<tr>
<td>DCO</td>
<td>18.0 mW at 4 GHz</td>
<td>11.4 mW at 2 GHz</td>
<td>54 mW at 32 GHz(^2)</td>
</tr>
<tr>
<td>Logic</td>
<td>15.6 mW at 4 GHz</td>
<td>8.3 mW at 2 GHz</td>
<td>15.9 mW at 32 GHz</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>0.5 GHz – 8 GHz</td>
<td>0.5 GHz – 4.4 GHz</td>
<td>24 GHz – 32 GHz</td>
</tr>
<tr>
<td>Phase Noise(^3)</td>
<td>-111 dBc/Hz at 4 GHz</td>
<td>-80 dBc/Hz at 2 GHz</td>
<td>-97 dBc/Hz at 32 GHz</td>
</tr>
</tbody>
</table>

\(^1\) ISSCC 2007, “A Wide Power-Supply Range (0.5V-to-1.3V) Wide Tuning Range (500 MHz-to-8 GHz) All-Static CMOS ADPLL in 65nm SOI”

\(^2\) Including the 1/16 pre-scaler and the output driver

\(^3\) At 1 MHz offset
Conclusion

• Modular All-Digital PLL architecture demonstrated on 4 different design points: 2 GHz (ring-DCO) and 6, 11 and 32 GHz (LC-DCO)
• Common core digital blocks shared between designs, easily mapped to different technologies
• Ring-DPLL tuning range and period jitter performance adequate for ASIC and microprocessor clocking applications
• LC-DPLL phase noise affected by limit cycle, typical of bang-bang digital PLLs