12.4 A 3.9ns 8.9mW 4×4 Silicon Photonic Switch Hybrid Integrated with CMOS Driver

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The emerging field of silicon photonics [1-3] targets monolithic integration of optical components in the CMOS process, potentially enabling high bandwidth, high density interconnects with dramatically reduced cost and power dissipation. A broadband photonic switch is a key component of reconfigurable networks which retain data in the optical domain, thus bypassing the latency, bandwidth, and power overheads of opto-electronic conversion. Additionally, with WDM channels, multiple data streams can be routed simultaneously using a single optical device. Although many types of discrete silicon photonic switches have been reported [4-6], very few of them have been shown to operate with CMOS drivers. Earlier, we have reported two different 2×2 optical switches wire-bond packaged with 90nm CMOS drivers [7,8]. The 2×2 switch reported in [7] is based on a Mach-Zehnder interferometer (MZI), while the one reported in [8] is based on a two-ring resonator.

In this work we report a 4×4 silicon photonic switch composed of 6 MZI based switches actuated by integrated p-i-n diodes. 6 waveguide crossings and 8 i/o fiber couplers as shown in Fig. 12.4.1. The switch is flip-chip bonded with a CMOS driver also shown in Fig. 12.4.1. Hybrid integration of photonic devices and controlling electrical circuits is an important step towards a full monolithic integration. It also offers significant advantages on its own by decoupling the optimization, fabrication and test of the optical and electrical components, increasing the design exploration space and shortening turnaround times. The driver shown in Fig. 12.4.1 is an all-static CMOS circuit, fabricated in a standard digital IBM 90nm process. The driver features an array of 6 output buffers, with predriver, controlled by a serial interface. Several versions of the driver chip have been designed and evaluated. All variants operate with ample speed (50ps to 100ps transition times) to drive ns-scale photonic switches. The photonic switch electrical load was modeled as a forward biased p-i-n diode. The diode model (Fig. 12.4.1) includes a series resistance, a charge-dependent capacitance and a current source of magnitude determined by carrier lifetime. The driver output of the 4×4 switch was tested, routing the 3×40 Gb/s signal from the East input to each of the 3 possible outputs, as shown in Fig. 12.4.6. Power sensitivity curves were taken for each state and each wavelength, demonstrating BER < 10^-12 at -10dBm average optical power. All wavelength channels and all configurations were found to be within a 0.5 dB power spread at a BER of 10^-11. Since each of the 2×2 switches dissipates 4mW in the ON state, the total power of the 4×4 switch depends on a particular routing state and can be as high as 16 mW, while 4 of the 6 MZI switches are turned on. Assuming uniform utilization of all 9 valid states and low frequency of routing state transitions, the average power of the 4×4 switch would be 8.9mW. Insertion loss of the switch was in the range from 3 to 6dB, depending on the routing state. Off-chip coupler loss was around 1dB. In all 9 valid states, the measured worst case crosstalk between channels was less than -10dB. The micrographs of the CMOS and the photonic dies are shown in Fig. 12.4.7. CMOS drivers with predrivers occupied 144×520µm^2. The total area of the 4×4 photonic switch was 300×1600 µm^2.

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References:

Figure 12.4.1: Block diagram of 4×4 photonic switch chip attached to CMOS driver chip.

Figure 12.4.2: Mach-Zehnder interferometer (MZI) based 2×2 switch.

Figure 12.4.3: Two-ring resonator based 2×2 switch.

Figure 12.4.4: Measured optical switching times of a 2×2 MZI switch.

Figure 12.4.5: Measured routing of 40 Gb/s data.

Figure 12.4.6: Measured routing of 3 × 40 Gb/s WDM data.
Figure 12.4.7: CMOS and Silicon Photonic die micrographs.