A new ultra-high sensitivity, low-power optical receiver based on a decision-feedback equalizer

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Motivation

• Goal:
Leverage CMOS complexity to improve sensitivity and to lower overall power dissipation of an optical receiver in a short reach optical communication link

• Key ideas of this work:
  – trade the transimpedance amplifier (TIA) bandwidth for sensitivity far beyond the traditional limits for a given data rate
  – use decision-feedback equalizer (DFE) to recover the bits from the TIA-induced deterministic eye closure, without broadband noise amplification
  – latches in the DFE replace limiting amplifiers, reducing overall power dissipation
In an standard OE module limiting amplifier (LA) and output stage (OS) bring the TIA output ($V_{TIA}$) to digital levels and drive $V_{OUT}$ over a short electrical link to the clocked chip.

In an integrated chip OS would not be needed.

LA can be removed as well: latches can make correct decisions with weak inputs (~10 mV at 10 Gb/s in 90 nm CMOS, after offset compensation).

Replacing LA and OS with a latch would save power, but what about sensitivity?
Increasing the gain of the TIA (RF) will boost the sensitivity, but it will also reduce the TIA bandwidth.

A short reach optical link is not introducing any significant loss or distortion – equalization is not required.

There is room then to apply equalization to a high-gain TIA itself, to treat it as a “channel”.

A peaking amplifier would not help with sensitivity since it amplifies high-frequency noise.

A heavy-duty (e.g., ADC-based) equalizer would dissipate too much power.
• Decision-feedback equalizer (DFE) does not amplify noise.

• DFE power dissipation can be low, depending on the channel.

• Smooth RC rolloff of the TIA can be compensated with a light 2-tap DFE.
1-tap Full Rate DFE Block Diagram

- DFE subtracts the post-cursor (tail from the previous bit).
- Feedback loop timing most challenging for 1\textsuperscript{st} tap at full rate.
- Half-rate clocking helps with feedback loop timing.
- Adding a 2\textsuperscript{nd} tap is straightforward, with small overhead.
CMOS Receiver Chip Block Diagram

- **VDD_TIA**
- **VDD_CORE**
- **S/H**
- **L1**
- **L2**
- **TIA**
- **BUF**
- **DAC**
- **SERIAL INTERFACE**
- **CMOS CHIP**

- **I_{PD}**
- **I_{REF}**
- **CLOCK**

- **2.8 kΩ**

- **25**

- **DAC**

- **I (µA)**
- **V (mV)**

- **Time (ps)**

- **V (mV)**

- **Time (ps)**
Die Image and Test Setup

- A 60 x 75 µm² receiver (core) in a 1.7 x 1.7 mm² padframe.
- With DACs (relaxed layout) area grows to 60 x 230 µm².
- On-chip testing infrastructure (clock receiver, output data drivers, serial interface) not included in area, power dissipation.
10 Gb/s, -25 dBm Bathtub Curve

- Horizontal eye opening: 36% at BER < $10^{-9}$.
- Same BER for PRBS7 and PRBS31 data patterns.
Power Sensitivity at 3 Gb/s and 4 Gb/s

- DFE taps: 1\textsuperscript{st} at 40%, 2\textsuperscript{nd} at 10% of the main tap.
- VDD\_TIA: 3.1mA, 1.0V; VDD\_CORE: 1.7mA, 0.9V (4.6mW total).
Summary

- A -25 dBm (1 A/W conversion) 1.2 pJ/bit 60 x 75 μm² (core) 4 Gb/s 90 nm CMOS optical receiver based on a new concept of processing TIA output directly with a DFE is demonstrated.

- This receiver can be used in highly integrated, massively parallel optical communication applications, enabling high density, low power links.
Backup Slides
A low power DFE can equalize a channel with bandwidth of one-tenth of the data rate. A 0.2 pF with an 800 Ω resistor will have 1 GHz bandwidth, good for 10 Gb/s.

The integrated noise on a 0.2 pF capacitor is 0.14 mV rms, or 180 µA rms of current noise. For BER < 10^{-12}, minimum input current is then 2.5 µA or -26 dBm (assuming 1 A/W conversion efficiency).