50Gb/s SiGe BiCMOS 4:1 Multiplexer and 1:4 Demultiplexer for Serial Communication Systems

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OUTLINE

☐ Motivation

☐ 4:1 Multiplexer Architecture

☐ 1:4 Demultiplexer Architecture

☐ Measurement Results

☐ Conclusion
Motivation

- SONET OC-768: next generation for long-haul optical transmission systems at 40Gb/s data rate
- Line rate can be as high as 50Gb/s when using FEC schemes
- Cost effective, low power ICs still need to be demonstrated
- SiGe BiCMOS technology good candidate?
Designs Overview

- Data rate target: 50Gb/s
- Half rate clocking
- Low supply voltage: -3.6V
- MUX/DMUX inputs/outputs data are unstaggered in time
- 0.18μm SiGe BiCMOS technology* with 120GHz $F_T$ and 100GHz $F_{\text{max}}$ NPNs

*A. Joseph, et. al., "A 0.18um BiCMOS Technology Featuring 120/100GHz (fT/fmax) HBT and ASIC-Compatible CMOS Using Copper Interconnect" Proc. BCTM, pp. 143-146, 2001
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4:1 Multiplexer
Block Diagram

D0

D2

Clock

D1

D3

Clock/2

Output
2:1 Multiplexer Timing

\[ t_{pd\_FF} < \frac{T_{ck}}{2} = 25\text{ps} \; @ \; 40\text{Gb/s} \]
Stage to Stage Timing

$t_{div} + t_{sel1} < T_{ck} = 50\text{ps} @ 40\text{Gb/s}$
Data Input Buffer

- **In**
- **Ref**
- **Out**
- **50Ω**
- **Gnd**
- **-3.6V**
Clock Input Buffer

Ck_In → Input Buffer → Amp1 → Amp2 → Ck_Out

50\Omega
Data Output Buffer

In

Out

Gnd

Inductive peaking

50Ω

Shunt capacitor

-3.6V
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1:2 Demultiplexer
Block Diagram

Data

Clock

D1

D0
Chips Photographs

4:1 MUX
(1.7x1.7mm²)

1:4 DMUX
(1.7x1.7mm²)
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MUX and DMUX Testing

- On-wafer
  - PPG used limited to ~14Gb/s
  - BERT used limited to ~13Gb/s
  - BER of MUX / DMUX checked at low speed
  - MUX switching behavior tested up to 56Gb/s
  - DMUX BER checked at 12.5Gb/s with 25GHz clock (corresponds to 50Gb/s operation)

- Packaged MUX and DMUX enabled BER testing at speed
On-Wafer 4:1 MUX Testing

- $V_{ee} = -3.3V$
- $2^{31}-1$ PRBS
- $T = 25^\circ C$

56 Gb/s: test equipment maximum speed
Package Description

- Gold ribbon bonds
- Alumina, $\varepsilon_r=9.8$
- Gold metalization
- Ground
- Signal
- Ground
- Ceramic
- Alumina/Graphite housing
- 12 mil
Package Photograph

V-connector

Feed-through with internal cap

1.95 x 1.75 inch

CPW transmission line
4:1 MUX Measurement Results

20GHz input clock

40Gb/s eye-diagram (on wafer, 100°C)

40Gb/s eye-diagram (packaged sample)
Back-to-Back MUX/DMUX Test Setup

- PPG
- Packaged 4:1 MUX
- Packaged 1:4 DMUX
- BERT
- Clock Source
- Delay Line

Signals:
- 4x10Gb/s 2^{31}-1 PRBS
- 1x40Gb/s 2^{31}-1 PRBS
- 10GHz
- 20GHz
Back-to-Back MUX / DMUX Testing

1:4 DMUX outputs at 10Gb/s

Horz: 20ps/div
Vert: 100mV/div

40Gb/s error free operation \( (BER < 10^{-15}) \)
Back-to-Back MUX / DMUX Testing

50Gb/s 4:1 MUX output

100 mV/div

5 ps/div

50 mV/div

20 ps/div

12.5Gb/s 1:4 DMUX output

50Gb/s error free operation (BER<10^{-15})
## Measurement Summary

<table>
<thead>
<tr>
<th></th>
<th>4:1MUX</th>
<th>1:4DMUX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal supply voltage</td>
<td>-3.6V</td>
<td>-3.6V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.47W</td>
<td>1.55W</td>
</tr>
<tr>
<td>Core power consumption</td>
<td>0.93W</td>
<td>0.93W</td>
</tr>
<tr>
<td>Max speed (BER&lt;10^{-15})</td>
<td>52.2Gb/s</td>
<td>52.2Gb/s</td>
</tr>
<tr>
<td>Clock phase margin@40Gb/s</td>
<td></td>
<td>11ps (44%)</td>
</tr>
<tr>
<td>Clock phase margin@50Gb/s</td>
<td></td>
<td>6ps (31%)</td>
</tr>
</tbody>
</table>
Conclusion

✓ Demonstrated up to 52.2Gb/s 4:1 Multiplexer and 1:4 Demultiplexer ICs (first pass success)

✓ Successfully packaged ICs enabled bit error rate testing at speed

✓ SiGe BiCMOS technology suited for high speed wired communication applications