A 0.18µm SiGe BiCMOS Receiver and Transmitter Chipset for SONET OC-768 Transmission Systems

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OUTLINE

- Motivation
- Receiver (Rx)
  - Architecture
  - Measurement
- Transmitter (Tx)
  - Architecture
  - Measurement
- Back-to-back Rx/Tx test
  - Packaging and test set-up
  - Measurement
- Conclusion
Motivation

✓ 4:1 MUX and 1:4 DMUX in 120GHz $F_T$ 0.18µm SiGe BiCMOS technology demonstrated at data rates to 50Gb/s and beyond (ISSCC’02)
✓ Half-rate architecture choice validated

→ Demonstrate 43Gb/s Rx and Tx chip set for OC-768 applications with 8% FEC coding
Challenges

- More complex high speed ICs
  - Clock distribution (especially for the Rx)
  - Power consumption
  - VCOs
- Jitter generation (Rx/Tx), tolerance (Rx)
- Half-rate architecture: clock duty cycle issue
  - Tx: output data duty cycle distortion
  - Rx: jitter generation/tolerance degradation
- Low supply voltage: -3.3V to -3.9V
- Up to 100°C chip temperature
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Rx Design Overview

- Includes:
  - Limiting amplifier
  - Clock and Data Recovery (CDR) unit
  - 1:4 demultiplexer circuit
  - Automatic frequency acquisition aid
  - Lock detector indicator

- Half-rate CDR architecture with on-chip loop filter

- Half-rate quadrature CMOS LC-VCO

- Supports two reference clocks: C16 and C64
Half-Rate Bang-Bang Phase Detector
Phase Detector 3-Level Generation

From transition detector

From phase detector output

3-level output
Quadrature CMOS LC-VCO
On-wafer Rx Measurement Summary

- Power supply: -3.3V to -3.9V
- Power dissipation @ -3.6V: 2.4W
- Tested error-free up to 100ºC chip temperature
- Input sensitivity @ BER<10^-9: 40mV
- Quadrature CMOS LC-VCO :
  - Total frequency range: 19.7GHz to 21.9GHz
  - VCO locking range: ~700MHz
  - Free-running phase noise at 1MHz offset: -103dBc/Hz
  - Temperature sensitivity: 1.9MHz/ºC
  - Supply voltage sensitivity: 133MHz/V
- Locked VCO clock jitter generation better than 230fs rms (1kHz-1GHz integration bandwidth)
Free-Running Rx VCO Phase Noise
Rx Phase Noise Plots

Carrier Freq 10.75 GHz Signal Track On DANL Off Trig Free
Log Plot

Marker 1.02942 MHz

Carrier Power -9.60 dBm Atten 0.00 dB Mrk2 1.03270 MHz
Ref -50.00 dBc/Hz
-109.25 dBc/Hz

Frequency Offset
1 kHz 1 GHz

Free-running VCO
Locked VCO
Reference

Marker Trace Type X Axis Value
1R 2 RMS Jitter 1.02 kHz -100.78 dBc/Hz
1A 2 RMS Jitter 1000 MHz 229.421 fs
2 3 Spot Freq 1.038 MHz -109.25 dBc/Hz

43Gb/s input eye diagram with added jitter (single-ended input)

Vert. 100mV/div, Horz. 12ps/div
11.3ps p-p jitter
1.2ps rms jitter (corrected)

Vert. 100mV/div, Horz. 50ps/div
Rx Chip Microphotograph

2.17mm x 2.17mm

Limiting Amp.

Phase Detector

2:4 DMUX

VCO

Loop Filter Capacitor
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Tx Design Overview

- Includes:
  - 4:1 multiplexer
  - Half-rate Clock Multiplier Unit (CMU)
- Conventional CMU using PLL technique
- On-chip half-rate bipolar LC-VCO
- Off-chip loop filter
Tx Block Diagram

4x10.75Gb/s single-ended data input

2.6875GHz Clock

Phase/Freq Detector

Charge pump

Linear amp

VCO

CLK

Data input buffers

4:1 MUX

Data output buffer

43Gb/s serial output data

CLK/8

CLK/2

Divider

CMU

Clock output buffer

21.5GHz

Off-chip loop filter

External Trim. bits

Data input buffers

4:1 MUX

Data output buffer

43Gb/s serial output data

CLK/8

CLK/2

Divider

CMU

Clock output buffer

21.5GHz

Off-chip loop filter

External Trim. bits
On-wafer Tx Measurement Summary

- Power supply: -3.3V to -3.9V
- Power dissipation @ -3.6V: 2.3W
- Tested error-free up to 100°C chip temperature
- Bipolar LC-VCO:
  - Total frequency range: 20.2GHz to 22GHz
  - VCO locking range: 600MHz
  - Free-running phase noise at 1MHz offset: -100dBc/Hz
  - Temperature sensitivity: 3.5MHz/°C
  - Supply voltage sensitivity: 190MHz/V
- Loop bandwidth: ~3MHz
- Jitter generation better than 170fs rms (10kHz-1GHz integration bandwidth)
- Jitter generation as low as 140fs rms under typical conditions (-3.6V, room temperature)
Tx Phase Noise Plots

SSB clock phase noise (dBc/Hz)

Frequency offset from carrier (Hz)

-180 -160 -140 -120 -100 -80 -60 -40

Free-running VCO
Locked VCO
Reference

43Gb/s Tx Output Eye Diagram

200mV/div

10ps/div
Tx Chip Microphotograph

1.7mm x 1.7mm
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Packaging

- 1.75”x1.95” ceramic substrate with 50Ω coplanar transmission lines
- V-connectors
- Ribbon bonds from chip to substrate
- Aluminum/Graphite housing
- Feed-throughs with internal decoupling caps + SM caps on selected power lines

- 1”x1.2” Arlon substrate with 50Ω microstrip transmission lines
- GPPO connector
- Ribbon bonds from chip to substrate
- Brass housing
- 100nF decap on all power lines
Back-to-Back Tx/Rx Test Set-Up

- **Pulse Pattern Generator**: 4x 10.75Gb/s 2\(^{31}-1\) PRBS
- **Packaged Tx**: Synthesized Clock at 10.75GHz, 1x 43Gb/s 2\(^{31}-1\) PRBS
- **Packaged Rx**: Recovered Clock at 10.75GHz, 4x 10.75Gb/s 2\(^{31}-1\) PRBS
- **Bit Error Rate Tester**: Reference Clock #1 at 2.6875GHz, Reference Clock #2 at 2.6875GHz

Note: clock#1 and clock#2 are not synchronized

Packaged Tx Output Eye Diagram

- 43Gb/s output eye diagram of packaged 4:1 MUX
- < 600fs rms jitter at eye crossing
- 500mV amplitude

Vert. 100mV/div, Horz. 5ps/div
Rx Input and Output Eye Diagrams

43Gb/s input eye diagram with added jitter (single-ended input)

One demultiplexed eye diagram

Vert. 75mV/div, Horz. 10ps/div
9ps p-p jitter
1.4ps rms jitter

Vert. 150mV/div, Horz. 19.1ps/div
Conclusion

✓ Demonstrated a 43Gb/s Receiver & Transmitter chipset implemented in 0.18μm SiGe BiCMOS technology
  ➡ Low jitter generation (230fs Rx, <170fs rms Tx)
  ➡ Good jitter tolerance demonstrated (system level measurement required)
  ➡ Low supply voltage (-3.6V) and power consumption (2.4W Rx, 2.3W Tx)

✓ Tested packaged Rx & Tx in a back-to-back configuration

✓ Half-rate Rx & Tx architecture suitable for OC-768 transmission systems