Organic Packages with Embedded Phased-Array Antennas for 60-GHz Wireless Chipsets

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***Abstract*— A multilayer organic package with embedded 60-GHz antennas and fully integrated with a 60-GHz phased-array transmitter or receiver chip is demonstrated. The package includes sixteen phased-array antennas, an open cavity for housing the flip-chip attached RF chip, and interconnects operating at DC–66 GHz. The 28 mm × 28 mm ball grid array package is manufactured using printed circuit board processes and uses a combination of liquid-crystal polymer and glass-reinforced laminates, allowing excellent 60-GHz interconnect and antenna performance. The measured return loss and gain of each antenna from 56 to 66 GHz are ∼10 dB and ∼5 dBi, respectively. Finally, the packaged transmitter and receiver chipsets, each working with a heat sink, have demonstrated beam-steered, non-line-of-sight links with data rates up to 5.3 Gb/s using 16-quadrature amplitude modulation single-carrier and orthogonal frequency division multiplexing schemes.**

***Index Terms*— 60 GHz, antenna-in-package, millimeter-wave package, phased-array antennas.**

I. Introduction

THE 60-GHz band supports multi-Gb/s wireless communication, leveraging the large amount of available and unlicensed bandwidth (7 GHz in most geographies). Potential large-volume applications of 60-GHz technology include uncompressed high-definition (HD) video streaming and wireless docking stations for laptops. These applications require non-line-of-sight (NLOS) wireless communications at 3 to 5 Gb/s over ranges of 5 to 10 meters using >1-GHz channel bandwidth. Unfortunately, achieving these requirements at 60 GHz requires higher gain antennas (>15 dB per side), since free-space path loss is inversely proportional to λ^2. Phased arrays are therefore being developed for these NLOS 60-GHz links, as they provide higher antenna gain together with beam-steering capabilities.

For the 60-GHz market to flourish, both low-cost semiconductor and low-cost antenna and packaging solutions are required. The recent advances in CMOS and SiGe technologies have enabled low-cost semiconductor solutions. Both single-element [1]–[3] and phased-array transceiver chipsets [4]–[6] have now been demonstrated. Turning to antennas and packaging, multiple single-element, fixed-beam solutions have been demonstrated at 60 GHz [7]–[9], however, little work has been published on cost-effective 60-GHz phased-array antennas and packages.

The 5-mm free-space wavelength at 60 GHz allows low-gain antennas to be embedded within a package or integrated on a chip (albeit with lower gain and radiation efficiency [10], [11]). Higher gain or phased-array antennas are more suitable for antenna-in-package (AiP) solutions, due to their larger area consumption. The incorporation of phased-array antennas into a package is not a trivial task due to the following: 1) the devised packaging solution should be compatible with mainstream manufacturing and assembly processes to capture high-volume markets; 2) the package materials and layer stack-up must enable excellent RF performance at 60-GHz while also being mechanically reliable; and 3) the physical structure of the package (interconnects, supply planes, cavities, etc.) should support the I/O and heat-removal requirements of the encapsulated integrated circuit (IC) while not degrading the antenna performance.

In this paper, we present a low-cost 60-GHz AiP solution that uses standard organic printed circuit board (PCB) processes and flip-chip technology. Section II discusses package design considerations including material selection and package structure. Section III describes technical challenges and proposed solutions in the fabrication and assembly of the package. Section IV discusses experimental results from a bare package as well as from an assembled module evaluated in an anechoic chamber. Section V discusses antenna and array performances related to manufacturing tolerance and array layout. Finally, Section VI summarizes the results.

II. Package Design

A. Materials

Multiple fixed-beam AiP implementations have been demonstrated using low temperature co-fired ceramic (LTCC) technology because it offers low-loss dielectrics and conductors, good thermal conductivity, and a high degree of integration due to cavities and embedded passives [8], [12], [13]. Although excellent 60-GHz antenna and interconnect performance can be achieved in LTCC, lower cost packaging technology is desirable.

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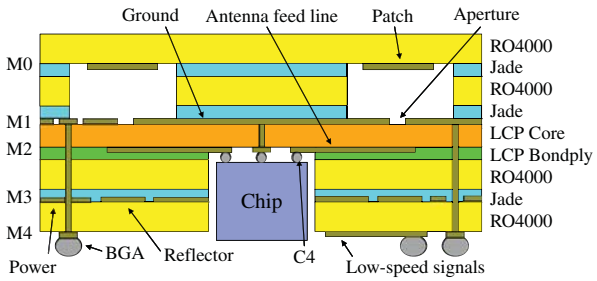

Fig. 1. Stack-up of the proposed flip-chip ball grid array (BGA) package.

Liquid-crystal polymer (LCP) has emerged as a promising low-cost alternative for millimeter-wave packaging material due to its unique electrical and mechanical characteristics [14]. A cross-sectional view of the proposed package is shown in Fig. 1. It has an LCP core surrounded by woven-glass-reinforced laminates (RO4000 series). An open cavity at the bottom accommodates the flip-chip attached die, avoiding potentially high-loss 60-GHz via structures [15]. An annular cavity is located underneath antenna patches, improving the antenna bandwidth and efficiency [16]. LCP was selectively used for antenna feed lines to have minimal insertion loss while RO4000 laminates with Jade adhesives were used elsewhere. Although the electrical properties of these materials were critical to the overall operation of the package and the antennas, they were unknown even to their manufacturers, and thus had to be measured using a cavity resonator and then fed back into electromagnetic (EM) simulations.

B. Antennas

It is challenging to achieve a 15% fractional bandwidth at 60 GHz. There have been two ways of tackling this challenge: one by using thick dielectric material and the other by using low dielectric constant material. Because a thick dielectric layer introduces more loss due to surface-wave excitation, and because low dielectric constant material such as Teflon leads to a mismatch in thermal expansion, more attention has been devoted to superstrate-covered cavity-backed antennas [16]. In Fig. 1, an air cavity between an antenna and a ground plane improves bandwidth and radiation efficiency by lowering the effective dielectric constant. Although the introduction of embedded air cavities poses manufacturing challenges, particularly if mainstream PCB processes are to be used along with high-performance RF laminates, the performance benefits conferred by the cavities are significant enough to warrant the required process development.

Aperture-coupled feeding allows that high-speed interconnects are routed below the ground plane and thereby decoupled from antenna patches. Apertures are designed to resonate at 60 GHz, thereby improving the antenna bandwidth further. The power plane beneath the apertures reflects backside radiation. More discussion on the antenna design can be found in [17].

C. 60-GHz Interconnects

While the prototype reported in [17] contains antenna components only, the final package also contains power distribution networks (PDNs) on metal layers M1 and M3, 60-GHz interconnects and other high-speed signals on M2, and low-speed signals on M4 (see Fig. 1 for notation). The overall dimension of the package is 28 mm $\times$ 28 mm $\times$ 1.2 mm with 288 balls.

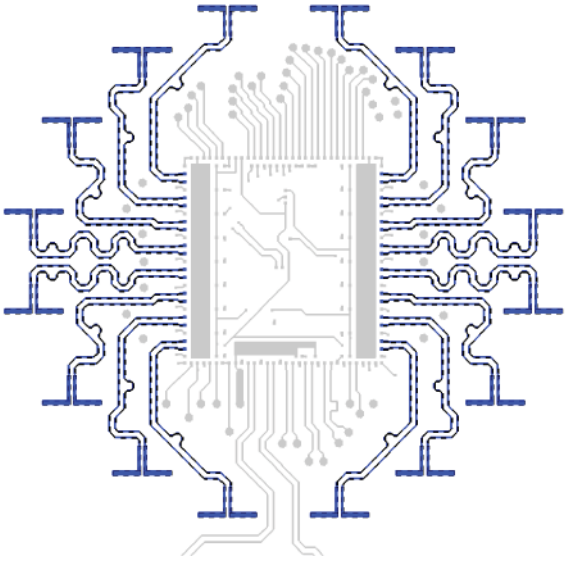

Fig. 2. Symmetric layout of 60-GHz interconnections (highlighted in blue) in Tx package.

One structure that had to be carefully optimized was the flip-chip transition structure as it directly affects the antenna bandwidth. A comprehensive sensitivity analysis [18] was conducted to optimize the controlled collapse chip connect (C4) joint, including pad size and pitch, bump diameter and height, and pad configuration (e.g., GSGSG versus GSSG in case of differential signaling). To summarize the results, a smaller pad with a larger pitch and a smaller bump diameter is generally preferable (listed in the order from the most to the least sensitive factor). Based on this, the diameter of bump limiting metallurgy pads on the chip surface was set to 100 μm, the lower spec limit of the technology, and the same value was used for package side pads. Although there are an increasing number of PCB manufacturers who can yield 75-μm wide traces, 100-μm traces were used to better allow for the misalignment of a laser-defined solder mask film. The pad pitch was selected to be 250 μm for differential and 225 μm for single-ended high-speed signals while 200 μm was selected for low-speed signals to minimize chip size. The total number of solder joints was set to prevent excessive collapse during C4 assembly. Finally, once each of these dimensions was set to its optimal value, equivalent circuit models were extracted from EM simulation so that on-chip impedance matching circuits could be designed. For the other high-speed signals that needed to be connected to a board, through-hole vias and BGA solder balls were optimized for discontinuity cancellation [19].

Since 60-GHz antenna feed lines are the most important structures in this package, they were the first to be routed. They were designed to exhibit quadrant symmetry as shown in Fig. 2, while maintaining both intra- and inter-pair skews

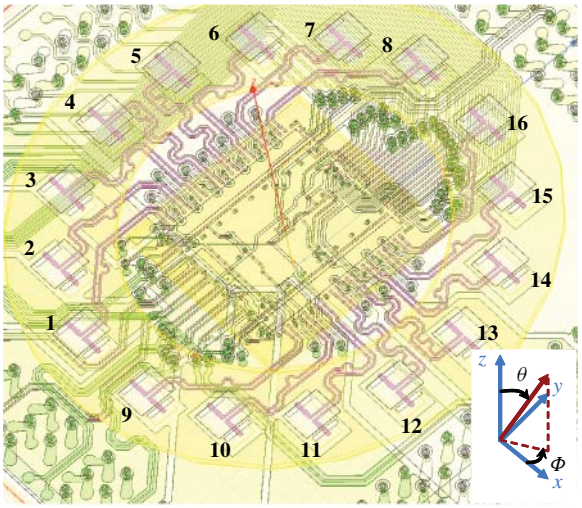

Fig. 3. HFSS model of Tx package (partly shown).

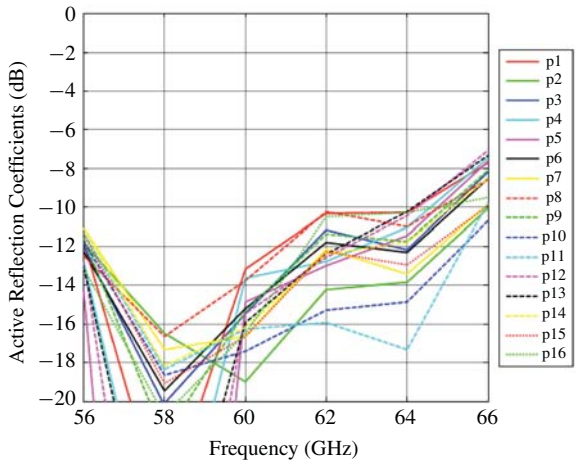

Fig. 4. Simulated reflection coefficients of 16 antennas in Tx package.

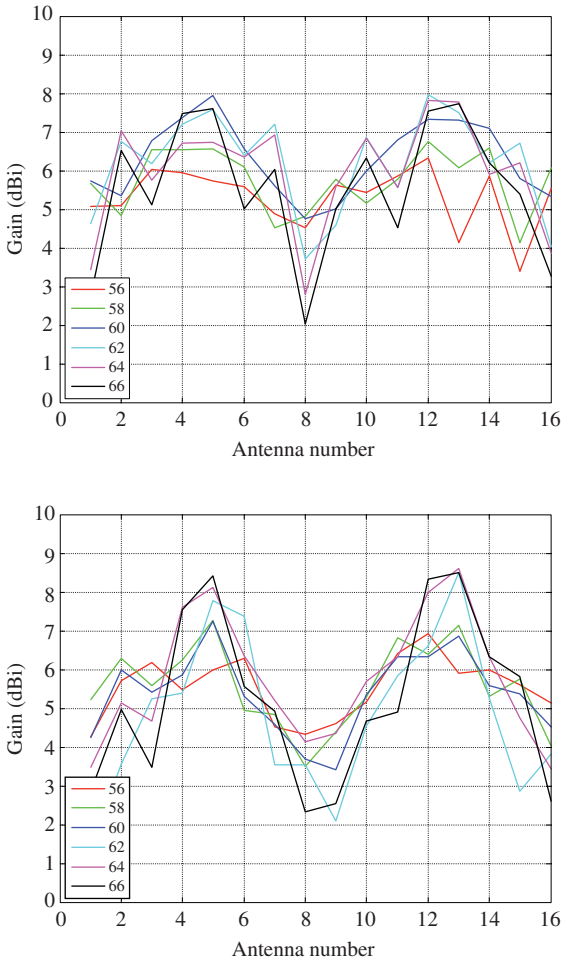

Fig. 5. Simulated antenna element gain at $\theta = 0°$ of, (top) Tx package (bottom) Rx package.

within 10° (∼75 μm). Although this requirement in physical length is enforced by a design rule check in a computer-aided design tool, it needs to be checked using 2.5-D simulation as propagation delay can vary significantly at meander bends. Several minor design revisions are usually required, and layout symmetry can reduce simulation time. The I/Q imbalance of FM and baseband quadrature signals had to be controlled even more tightly. Since some of these differential pairs were routed on a different layer due to space limitations, full 3-D simulation was conducted to accurately capture the behavior of multiple vias.

D. PDNs

Since there were only two metal layers (M1 and M2) above the chip cavity and M2 was heavily crowded with signal traces, several metal strips were carefully designed on M1 to connect each power pin to a corresponding power plane on M3. Since M1 was functioning as a reference plane for high-speed signals on M2, the strips had to be narrow enough not to cause return path discontinuity, and at the same time wide enough to avoid excessive inductance and resistance in PDNs. Every critical power domain was modeled using the transmission line method [20], which allowed various scenarios to be simulated in a short period of time.

E. Post-Layout Simulation

Once layout was completed, full 3-D simulation was conducted as a final verification. Fig. 3 shows the 2-D view of an HFSS model for the transmitter (Tx) package along with port labels (defined at C4 pads) and the coordinate system used. Fig. 4 shows the simulated return loss for each of the sixteen Tx antennas with all other ports terminated with 100 Ω. The return loss is better than 10 dB over the 60-GHz band (56–66 GHz), meeting the design objective. When the array beam is scanned off-axis (for θ between 0–30° and φ between 0–180°), the return loss is still better than 7 dB across the band.

Fig. 5 shows the simulated antenna element gain for just one particular direction, $\theta = 0°$, with different curves showing responses at different frequencies. Here, the gain of each antenna is computed with all other ports terminated with matched loads, and mutual coupling among the antennas is also included. Antenna gain is dependent upon its location, showing 2–8 dBi element gain across frequency with the average gain of ∼5.5 dBi. To understand this element-to-element

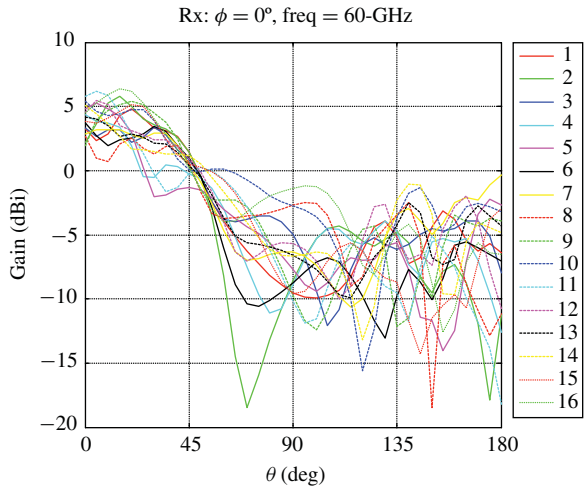

Fig. 6. Simulated array element pattern on the E-plane of Rx package.

gain variation, one must examine the radiation patterns of the sixteen individual antennas. One example is shown in Fig. 6 for the E-plane ($\theta = 30°$ and $\varphi = 0°$) at 60 GHz. It can be seen that the peak gains of some antennas point off-axis. Also note that Fig. 5 reveals a systematic pattern, where each quadrant of antennas exhibits the same location dependency. This will be further discussed in Section IV.

III. Package Manufacture and Assembly

The superior electrical performance of LCP comes with a cost. Since it has only recently been used in low-cost PCB processes, it was time-consuming to find the right recipe. One problem with many polymer materials, including LCP, is that they outgas during thermal bonding processes. Since the metal pattern on M1/M2 is quite complicated due to chip I/O escape, LCP/Jade adhesives sometimes fail to perfectly conform to the surfaces and end up with voids. Any gas trapped in the voids may explode when exposed to high temperatures, resulting in delamination or in more extreme cases, external blisters.

Delamination and blistering can mostly be avoided by applying higher pressure during press cycles and avoiding high temperature processes as much as possible. Once the package is built, the next challenge is the C4 reflow process. Since there was no known low-cost method of stencil printing eutectic solder cap inside the chip cavity, lead-free solders were used and the LCP core had to be exposed to the lead-free solder reflow cycle. In early manufacturing results, there were a few cases in which a fully tested chip was found to be non-functional after being packaged.

Considerable effort was also made to come up with a reliable flip-chip assembly process for mounting the chip in the package. First, the dimensions of the chip cavity need to be optimized. If the cavity is too large, a large portion of 60-GHz traces is exposed to underfill material whose loss tangent is typically an order of magnitude greater than that of LCP. On the other hand, if the cavity is too small, it is difficult to perform capillary underfill. In addition, the thickness of the solder mask should be controlled accurately to prevent joint open failure. Fig. 7 shows the first-of-a-kind multilayer organic package fully integrated with the 60-GHz phased-array IC.

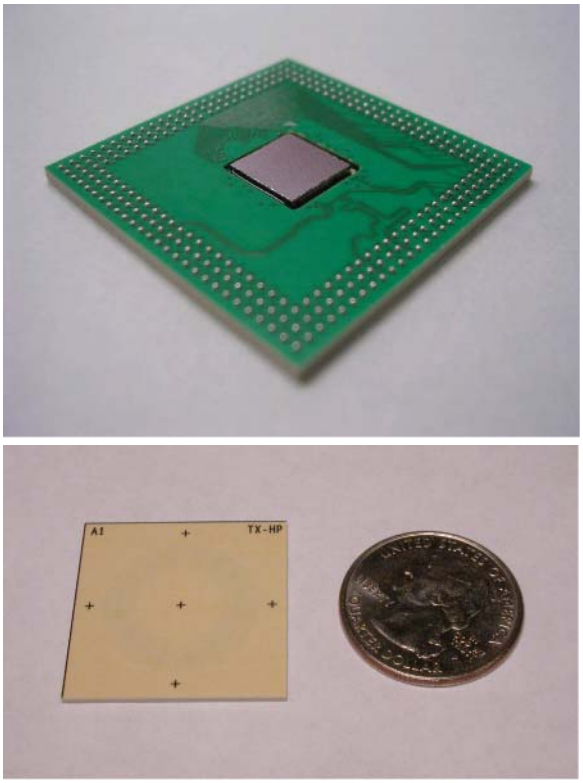

Fig. 7. First-of-a-kind multilayer organic package fully integrated with the 60-GHz phased-array IC.

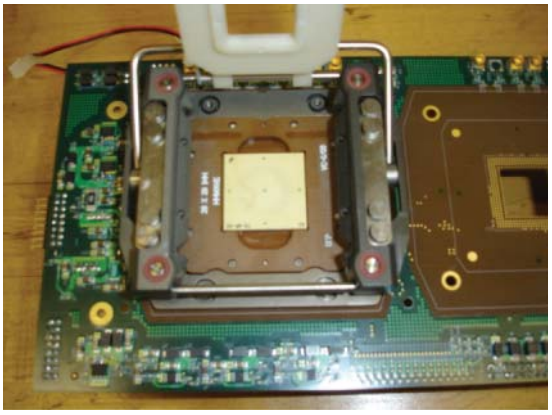

Fig. 8. Package mounted in test socket.

Assembled modules were first tested in a socket evaluation board as shown in Fig. 8. A high-speed pogo pin test socket allowed the assembled packages to be screened quickly by performing a digital test. Further tests monitored synthesizer locking, the voltage and current consumption of each power supply, and even the output power and radiation pattern of each antenna element. Note that the socket lid is made of a polymer with a center window, minimizing interference with the radiation pattern. Although not shown in the picture, a heat sink is spring loaded into a stiffener plate on the other side of the board to control chip temperature during the tests.

Screened modules were then soldered down to the evaluation board for detailed antenna measurements. Although the power consumption of the chipset is only 2–4 W [4], [5], it

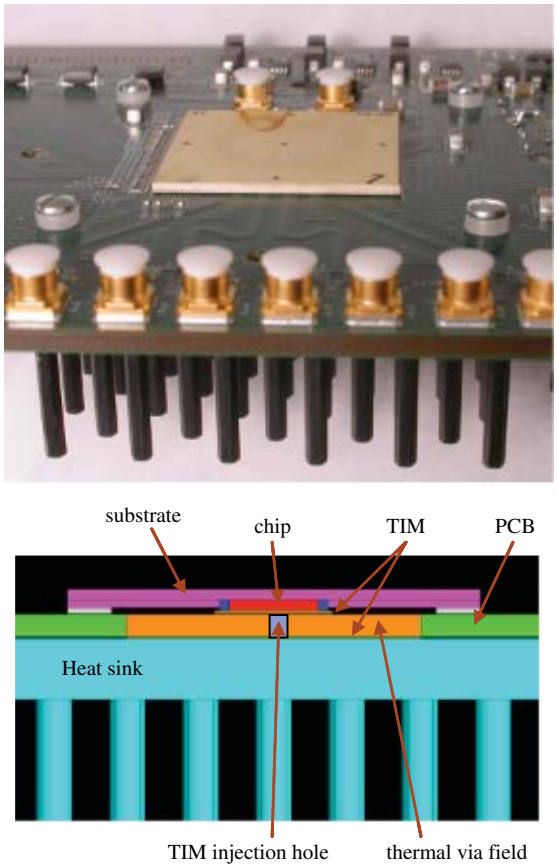

Fig. 9. Package mounted on evaluation board with heat sink.

is not easy to dissipate because of space limitations and the high ambient temperature in some applications (e.g., plasma HDTV displays). Fan cooling was considered unacceptable. In addition, a heat sink should not interfere with the antennas. A devised cooling solution is shown in Fig. 9. After BGA reflow (and subsequent surface mount device reflow), a thermal interface material (TIM) was injected through a via hole from the back side of the board using a syringe. In this way, the TIM can be injected near the very end of the assembly process and need not be exposed to solder reflow conditions several times. Otherwise, an extensive production qualification test would be required to confirm TIM stability before going into production. Since the heat sink is mounted on the opposite side of the board from the package, it does not affect the antenna performance.

It was observed from simulation that the TIM accounts for a considerable portion of overall thermal resistance unless it is thin enough. Therefore, BGA stand-off should be minimized, but it needs to remain large enough for TIM injection to remain viable. The following parameters (and their tolerance) need to be considered: ball size, cavity depth, die thickness, via hole size, and the viscosity of the TIM. By exercising precise stand-off control, the overall thermal resistance can be kept below 10–15 °C/W depending on the size of a pin-fin heat sink.

IV. Package Characterization

Several bare packages were measured by wafer probing prior to flip-chip assembly. Fig. 10 shows the comparison of

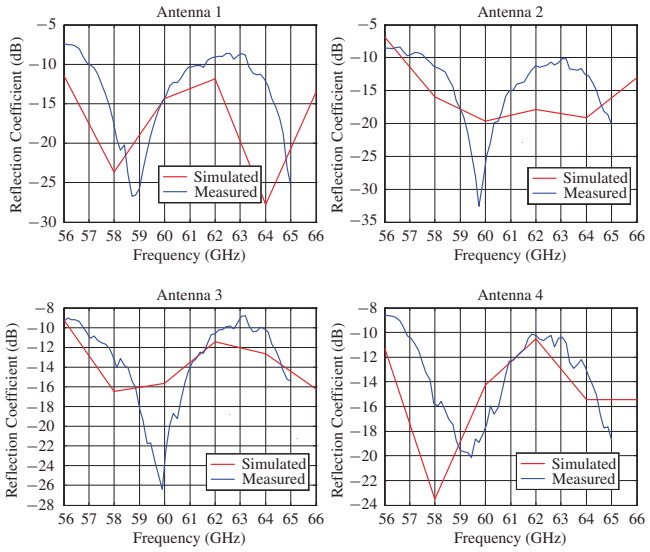

Fig. 10. Comparison of simulated and measured reflection coefficients, antennas 1−4 of Rx package.

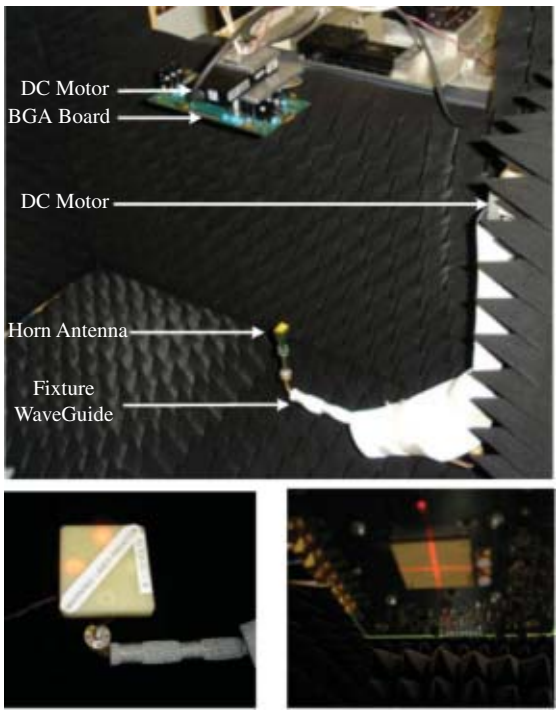

Fig. 11. Assembled module measured in anechoic chamber using automated testbed fixture.

the measured and simulated reflection coefficients of Rx antennas. Despite the fact that in the measurement all remaining antenna ports were open, good model-to-hardware correlation is observed because coupling among the antennas is weaker than −17 dB. Part-to-part variation was also minimal.

Screened modules (after flip-chip assembly) were soldered down to the evaluation board and measured in an anechoic chamber using an automated testbed fixture, as shown in Fig. 11. Two DC motors allow the antennas to be characterized across θ and ϕ. The horn antenna has ∼20 dB gain and the distance between the module and the antenna is 38 cm (corresponding to approximately 60 dB of path loss). The net

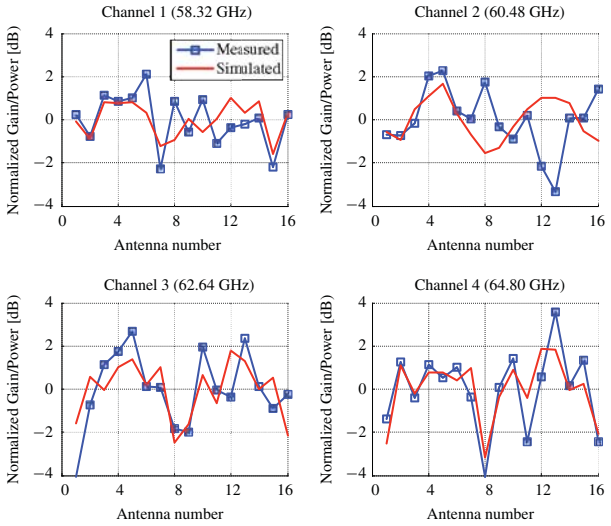

Fig. 12. Comparison of simulated and measured antenna gain of Tx package.

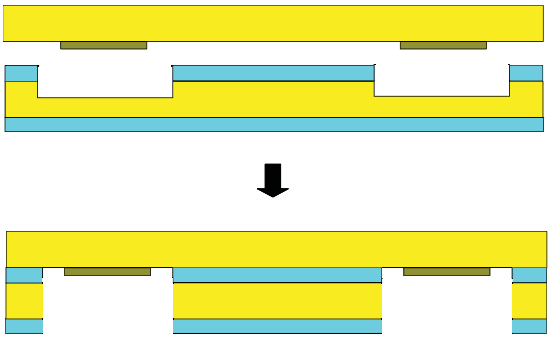

Fig. 13. Substrate and cavity manufacturing flow.

total loss, including the cable loss, waveguide loss, antenna gain, and path loss is roughly 50 dB. For alignment purpose, a laser assembly is placed on top of the horn antenna as shown in Fig. 11 (bottom left). It creates two beams that are aligned to the marks on the package as shown in Fig. 11 (bottom right).

Fig. 12 shows a comparison of the simulated gain and measured power of the 16 Tx antennas over the four IEEE channels. For comparison purposes, both the simulated antenna gain and the measured output power have been normalized to their average value. Note that the simulations were performed at 58, 60, 62, and 64 GHz, which are slightly different from the four IEEE channels (58.32, 60.48, 62.64, and 64.80 GHz) at which the antennas were measured. Although the measurements also include the composite response of the chipset and the flip-chip transition, both results are in excellent agreement. Given the complexity of the EM models and the measurement setup, the degree of correlation is remarkable—validating both the EM simulation methodology and the 60-GHz measurement setup.

V. Issues Related to Antenna and Array Performance

The antenna and array performance is dependent on the package manufacturing tolerance, antenna air cavity dimensions, and array layout. Performance related to manufacturing tolerance has been studied in [17]. Due to the wideband nature, the antenna return loss and gain will not change much if the depth of the air cavity is within ±1 mil from the nominal 12 mil value [17]. Fig. 13 illustrates one way of implementing the air cavity. Cavity depth routing is performed twice, first from the top before tack bonding and then from the bottom after the bonding. In this way, high-precision depth routing (e.g., laser drilling) is not necessary and the manufacturing tolerance of the cavity depth is no greater than board thickness tolerance. The manufacturing tolerance in the horizontal dimension as much as ±4 mil will have almost no impact on the antenna performance.

Our circular array achieves −8 dB side lobe levels which are 5 dB higher than the −13 dB levels for the 16-element linear case. This difference is expected and is due to the ring

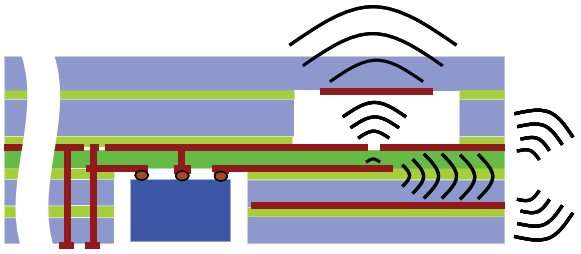

Fig. 14. Element-to-element antenna gain variation due to edge radiation.

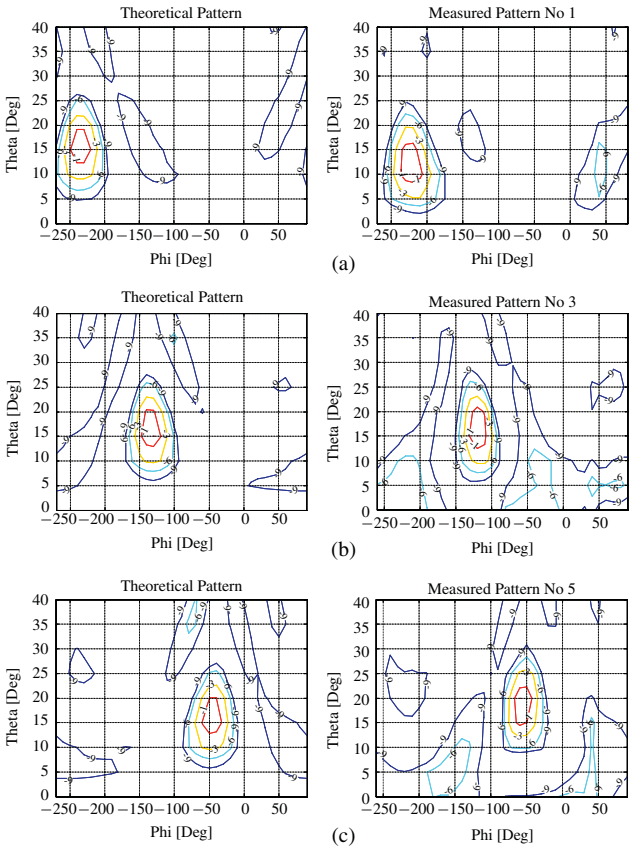

Fig. 15. 2-D, 16-element radiation patterns at 60.48-GHz in spherical coordinates for (a) Theta = 18° and Phi = −225°. (b) Theta = 18° and Phi = −135°. (c) Theta = 18° and Phi = −45°. Measured from a packaged Tx IC in an antenna chamber.

configuration which does not include antenna elements in the center [17], [21]. Despite the relatively higher side lobe levels, the ring configuration makes it easy to design equal length feed lines in the package environment (see Fig. 2). A relatively narrow beam width of element radiation patterns will also increase the array side lobe levels when the main beam is steered far away from the broadside direction.

One area for further improvement is element-to-element variation in antenna gain. The gain variation is caused mainly by three factors. First, it is a characteristic of finite arrays, which is, to some extent, inevitable [22]. A simple infinite-array theory cannot account for edge effects caused by the finiteness of the array and by a bounded ground plane. Radiation patterns or antenna gain can be strongly affected by nearby elements even when reflection coefficient is almost unaffected, and this may result in considerable difference in side-lobe level between finite-array behavior and the infinite-array approximation [23]. This effect can be mitigated by further separating the elements, at the cost of reduced scanning range. Second, the bounded ground plane, or finite ground plane, also perturbs the radiation pattern. As shown in Fig. 14, energy coming in along the antenna feed line also excites a parallel-plate mode in addition to being coupled to the patch through the aperture. The parallel-plate mode propagates toward the edge and then radiates into the air. Surface waves, existing in patch-related antennas as in the case here, have a similar effect. The main and edge radiations can interfere constructively or destructively depending on the location of each antenna and frequency. Study indicates that the element gain variation can be reduced if the package size is increased by about the half wavelength. Third, extensive simulations indicate that increasing the outer diameter of the ring air cavity will also reduce the element gain variation. The gain variation can be reduced to ± 1 dB by optimizing package size and ring diameter, and next generation packages are being designed in this way.

It should be noted that the variation across elements observed in the current modules can still be fully equalized by adjusting the gain and phase settings of the Tx/Rx IC [24], [25]. The element-to-element gain and phase variations are taken into account when the beam table (see [24]) is synthesized to achieve desired beam direction. Therefore, actual array performance will not deviate much from ideal array performance as long as the element-to-element variation is systematic and within the programmable gain range (10 dB) and the phase-shift range ($>360°$) of the power amplifier. Fig. 15 compares the measured and the ideal 2-D radiation patterns for different sets of element weights. The ideal patterns assume sixteen identical elements and isotropic antennas. The good match between theory and measurement shows successful 16-element beam forming in the module. These exemplary beams are general and were designed without any special considerations for side-lobe suppression or notch in a particular direction.

VI. Conclusion

For the first time, an organic package with embedded antennas and fully integrated with a 60-GHz phased-array IC has been demonstrated. In spite of numerous challenges in design, manufacturing and assembly, first-pass fully functional packages were delivered. With effort, excellent model-to-hardware correlation has been achieved in the EM simulation of complex antenna systems. The measured phased-array beam patterns have demonstrated beam-steering capability across all four IEEE 802.15.3c channels. In preliminary link experiments with the Tx and Rx modules, a 5.3 Gb/s OFDM link has been achieved in each of the four IEEE channels with 4-m Tx-Rx separation (limited by lab space) [5]. Measurements have also been performed to verify the ability of the array to set up alternate paths when the LOS between the Tx and Rx is blocked. NLOS HD wireless video links (1 080p resolution) using all sixteen receive and transmit array elements have been achieved with total path length of 20 m (using single reflection off a wall), demonstrating the beam steering and beam forming ability of the phased-array chipsets. By adopting standard organic PCB process and flip-chip BGA technology, this low-cost AiP solution paves the way for the market success of millimeter-wave applications.

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