MIEC (mixed-ionic-electronic-conduction)-based access devices for non-volatile crossbar memory arrays
Invited Review

MIEC (mixed-ionic-electronic-conduction)-based access devices for non-volatile crossbar memory arrays

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Abstract

Several attractive applications call for the organization of memristive devices (or other resistive non-volatile memory (NVM)) into large, densely-packed crossbar arrays. While resistive-NVM devices frequently possess some degree of inherent nonlinearity (typically 3–30× contrast), the operation of large (>1000×1000 device) arrays at low power tends to require quite large (>1e7) ON-to-OFF ratios (between the currents passed at high and at low voltages). One path to such large nonlinearities is the inclusion of a distinct access device (AD) together with each of the state-bearing resistive-NVM elements. While such an AD need not store data, its list of requirements is almost as challenging as the specifications demanded of the memory device. Several candidate ADs have been proposed, but obtaining high performance without requiring single-crystal silicon and/or the high processing temperatures of the front-end-of-the-line—which would eliminate any opportunity for 3D stacking—has been difficult.

We review our work at IBM Research—Almaden on high-performance ADs based on Cu-containing mixed-ionic-electronic conduction (MIEC) materials [1–7]. These devices require only the low processing temperatures of the back-end-of-the-line, making them highly suitable for implementing multi-layer cross-bar arrays. MIEC-based ADs offer large ON/OFF ratios (>1e7), a significant voltage margin Vin (over which current <10 nA), and ultra-low leakage (<10 pA), while also offering the high current densities needed for phase-change memory and the fully bipolar operation needed for high-performance RRAM. Scalability to critical lateral dimensions <30 nm and thicknesses <15 nm, tight distributions and 100% yield in large (512 kBit) arrays, long-term stability of the ultra-low leakage states, and sub-50 ns turn-ON times have all been demonstrated. Numerical modeling of these MIEC-based ADs shows that their operation depends on Cu⁺ mediated hole conduction. Circuit simulations reveal that while scaled MIEC devices are suitable for large crossbar arrays of resistive-NVM devices with low (<1.2 V) switching voltages, stacking two MIEC devices can support large crossbar arrays for switching voltages up to 2.5 V.

Keywords: MIEC, access devices, nonvolatile memory, memristive devices
1. Introduction

A crossbar array consists of a dense, cartesian array of interconnections at the crossover points between two planes of closely-spaced wires running at right angles to each other. If both the wires and the spaces between them have width $F$, then the area per connection is $4F^2$. A crossbar memory device must be a two-terminal device that can be reliably, repeatedly, and readily switched between at least two resistance states, preferably with a large resistance contrast. This switching operation must not require excessive power, yet the device should be capable of surviving through many millions, if not billions or more, of switching cycles. Each read operation, at lower voltages and currents than the switching operation, needs to supply current sufficient for distinguishing the various states. Yet even a very large number of successive read operations must not induce a switching event.

Research over the past 10–15 years, originally motivated by the desire to have a ‘backup device’ in case either NAND or NOR Flash had trouble scaling to smaller dimensions, has produced a number of viable two-terminal non-volatile memory (NVM) devices [8–10], including memristive devices [11]. There has been a general realization that many of these two-terminal NVM devices might offer better performance than NAND Flash through much lower latencies and much higher program-erase endurance. This opportunity is referred to collectively as Storage Class Memory [8, 12].

Here we focus on the leap from a single, ‘state-holding’ memory device to a large array of memory devices. Ideally, within a vast matrix of densely packed devices, we would be able to write and read any small subset of the memory devices at will, yet all other devices would remain completely unperturbed, dissipating zero additional power beyond that required for writing or reading. We can come close to this ideal by introducing a strongly nonlinear $I-V$ characteristic—an access device (AD)—together with the state-bearing memory element at every crossbar node.

One way to introduce this nonlinearity is to integrate a second two-terminal device—such as a diode, switch, or other similar element—in series with each state-holding (NVM) element. These devices can each be optimized separately, and then integrated together in the final semiconductor processing scheme, though this may increase the number of processing steps. An alternative approach is to simply add the need for massive nonlinearity to the already long list of criteria that the prospective state-holding element must deliver. If successful, this approach leaves only one device to integrate; unfortunately, the criteria for state-holding devices is quite daunting already, without adding a strong nonlinearity of many orders of magnitude—at exactly the ‘right’ voltage—to the list.

In this review article, we briefly overview crossbar biasing schemes, and discuss the need to minimize leakage through various non-selected cells while delivering the right voltages and currents to the selected cell. After summarizing the list of criteria for an AD, we briefly review current research on various discrete AD options [13]. These include conventional silicon-based semiconductor devices, oxide semiconductor devices, threshold switch devices, oxide tunnel barriers, and various approaches for self-selected RRAM [13]. We then review our research on ADs based on mixed-ionic-electronic-conduction (MIEC) [1–7], and show that these devices are highly suitable for multi-layer crossbar memory for resistive-NVM devices with modest switching voltages.

Some figures may appear in colour only in the online journal.
2. Crossbar arrays

In a crossbar array, a set of voltages is applied at the edge of a given sub-array within the chip, such that the desired operations (reads and writes) take place at the desired selected cells, yet all un-selected cells remain unperturbed and overall power dissipation remains manageable. It can be readily shown [14] that it is nearly impossible to implement a crossbar array of any practical size without a strong nonlinearity at each node—we will not repeat such analyses here. Each sub-array should be as large as possible, to amortize the peripheral circuitry placed at the edge for rapidly driving the large writing currents and for accurately sensing the small read currents. The larger these sub-arrays, the larger the area efficiency: the fraction of silicon used for memory bits, and such higher area efficiency typically leads to a lower cost-per-bit.

While there is a strong incentive to make sub-arrays as large as possible, this must be traded off against the problems associated with large sub-arrays, including significant line capacitance, large worst-case resistance drop, and difficulties in enforcing compliance currents within the array [13]. A major issue is the aggregate leakage through all the devices other than those selected for write. Such leakage can be constrained by careful choice of the biasing scheme: the intermediate voltages that are applied to all the other wires within the array, so as to minimize the overall leakage and prevent any undesired disturbance to previously stored data.

As shown in figure 1, these other devices in the array fall into three classes: the half-selected devices along the same row as a selected device, the half-selected devices along the same column as a selected device, and the un-selected devices that share neither a row nor a column with any selected device. The ‘V/3’ scheme [14–17]—in which applied voltage is split into three parts, one for each of the three classes of non-selected devices—is highly useful when supplying large writing voltages to one or more selected devices. As shown in figure 1, the sum of these three voltage drops is roughly equal to the effective voltage drop across the selected device. While the name ‘V/3’ would suggest division into three equal voltages, it often makes sense to reduce the voltage across the many un-selected devices until total aggregate leakage is minimized (figure 1) [13].

During write operations, it is critical to deliver the necessary voltage and current to the selected cell while avoiding two undesirable outcomes: dissipating too much aggregate power, and risking even the remote possibility that any of the non-selected cells might accidentally switch. For large arrays, excess power dissipated during write may reduce the achievable write parallelism (and thus write bandwidth), and large sub-arrays lead to more aggregate leakage and larger \( \frac{1}{2}CV^2 \) energy for driving wires to the desired voltage levels.

During read operations, since both the currents and the associated device voltages are typically significantly smaller, a ‘V/2’ scheme can be used, where the voltage applied to the wires leading to un-selected devices is either brought to zero or alternatively, these lines are allowed to float [15, 18, 19]. During read, the strong nonlinearity at each node suppresses the many potential ‘sneak paths’ that could lead to inaccurate sensing of the state of selected devices.

A final consideration is the (hopefully) small fraction of ADs that fail in a low resistance, or ‘shorted,’ state. Such devices act just like strong ‘sneak paths,’ masking read currents from all devices that share the same sense-amplifier and dissipate significant power during write. One approach for combatting this problem, demonstrated for two-terminal MIEC-based ADs in series with phase-change memory (PCM) [3], is to place the state-bearing device (associated with the shorted AD) into an extremely high resistance state. This is possible for PCM because negative polarity pulses that are ramped down slowly are known to lead to phase-separation of the phase-change material [20, 21], producing a very high resistance state. Although this requires a voltage similar to very large writing voltages, this corrective action can be taken without damaging neighboring devices because the failed AD is not consuming any of the voltage drop. The NVM device, once in this ultra-high resistance state, then protects the array from the leakage that would otherwise be induced by the shorted AD. Unfortunately, it is not yet clear if other resistive-NVM devices besides PCM can be placed in such a high-resistance state with voltage sequences that can be applied within the array without damaging neighboring healthy device pairs.

3. AD requirements

An AD should be capable of a high ON-state current density, so it can supply high currents through its small cross-sectional area, as needed to program and erase memory elements. Since un-selected cells vastly outnumber the selected cells, the AD’s OFF-state leakage current needs to be as low as possible, so as to prevent the aggregate leakage through all the un-selected cells from dominating the overall system power budget. Satisfying both of these first two points (high ON-state current and low OFF-state leakage) simultaneously implies that the AD must have a highly nonlinear \( I-V \) curve.

Many resistive-NVM devices candidates either show better reliability, or only operate correctly, when program and erase pulses use opposite voltage polarities, requiring that the AD support bidirectional operation. Process compatibility with 3D multilayer stacking allows the AD, like most emerging resistive-NVM elements, to be located above the wafer surface without consuming active Si wafer area. This frees up Si area for placement of some peripheral circuits underneath the crossbar memory array, and enables multi-layer stacking of arrays if the AD (and NVM) can be fabricated in a back-end-of-the-line (BEOL)-compatible process. Such a process can involve prolonged and repeated exposures to temperatures of \( \sim 400^\circ \text{C} \), yet forbids processing at any temperatures significantly higher than this value.

The AD must achieve voltage compatibility with the memory element with which it is paired. If the AD’s turn-on voltage is much lower than that needed across the selected memory element, array biasing voltages will lead to large
currents through the half-selected cells, degrading the effective selectivity and ON/OFF ratio of the ADs [7]. All other properties of the AD should be better than or equal to that of the memory element, so that its switching speed, cycling endurance, array yield, and variability do not limit the performance of the resulting memory chip.

4. Other proposed ADs

The set of requirements listed above have made it very challenging to find ADs that are fully suitable for high-density, 3D multilayer resistive crossbar memory [13].

After decades of research and development, Si-based ADs are very well understood. However, three-terminal devices are non-trivial to implement in a 4F^2 footprint, and devices that require single-crystal silicon preclude 3D multilayer stacking. Polysilicon devices can be stacked, but typically require high (>400°C) fabrication temperatures [13].

The main advantage of oxide PN junction ADs is their low fabrication temperature, providing compatibility with 3D multilayer stacking approaches. ADs based on metal-oxide Schottky barriers offer both relative ease of integration and low (<400°C) processing temperatures. However, the ON-state current density of both oxide PN junctions and metal-oxide Schottky barriers needs improvement by several orders of magnitude for operation with most resistive memory elements [13]. Both Si rectifiers and oxide PN junction diodes support only unipolar operation, and will not work with bipolar memory elements. However, it is possible to get bidirectional operation using Si NPN punchthrough diodes [22] or metal-oxide-metal Schottky barrier devices with appropriately chosen metal electrodes [23, 24].

Three types of threshold switches have been proposed as potential ADs for resistive-NVM devices [13]: ovonic threshold switching (OTS) devices [25], Metal-insulator transition (MIT)-based devices [26, 27], and the threshold vacuum switch (TVS) [28]. OTS devices have been shown with good switching performance and in large arrays [25], but require complex materials and improvements in switching endurance and leakage current will be needed. It is also not yet clear what sort of RRAM switching voltages and state resistances which OTS or other threshold ADs might be able to accommodate.

In contrast, MIT and TVS switches have been demonstrated only at the few-device level, both individually and in series with RRAM devices. While MIT devices using materials such as NbO₂ with acceptably high threshold temperatures have been demonstrated [27], it will be important to further reduce the half-select and un-select leakage currents. Also, higher threshold temperature implies that added electrothermal power is being used to trigger the MIT behavior, which could potentially increase the overall power required for NVM switching. The TVS device [28] is interesting, but it will be critical to demonstrate that sufficiently identical vacuum gaps, leading to tightly distributed electrical switching characteristics, can be demonstrated at high yield over large arrays of TVS ADs.

Oxide tunnel barriers offer steeply nonlinear curves, and have attained success in combination with various memories including conductive-bridging RAM (CB-RAM) and non-filamentary conductive metal oxides [29, 30]. However, it is extremely important that the switching voltages of the RRAM remain low so that the half-select leakage—as evaluated at a half (or in the ‘V/3’ scheme, at roughly a third) of the applied voltage across both memory and AD, as well as across any extra bias dissipated in the wiring—can still be low.

Methods for adding AD functionality to resistive-NVM devices [13] include the complementary resistive switch (CRS) [31], hybrid devices in which AD functionality is incorporated together with the memory functionality [32, 33], and nonlinear RRAM, in which barrier layers introduce nonlinearity to help reduce leakage current [34–37]. Although a CRS device can significantly reduce sneak-path currents, destructive readout with subsequent write-back is required. In addition, each CRS device must either be fabricated from a stack of two well-behaved and symmetric memory elements [31], or a single RRAM layer with very precise control over operating voltages [38, 39]. A particularly important step will be the demonstration of reliable CRS operation at the low switching currents (20–50 µA) required for implementation in the narrow-pitch wiring of advanced technology nodes [19].

Another aspect of self-selected memories is the difficulty in independently tuning select-device and memory functionality. This is more of an issue in hybrid devices using MIT or tunnel barriers which participate in the motion of oxygen ions, since the select function is nearly inseparable from the memory function. While nonlinearity can be tuned by increasing the thickness of an added tunnel barrier, the maximum nonlinearities achieved so far fall well short of the large (10^5–10^6) values needed for large (1000 × 1000) sub-arrays [35, 37].

5. MIEC

BEOL-friendly AD based on Cu-containing MIEC materials [1–5] have become an intriguing choice as 3D-ready ADs for NVM. MIEC-based ADs offer large ON/OFF ratios (>10^5), high voltage margin V₉ (over which current <10 nA), and ultra-low leakage (<10 pA), while also offering the high current densities needed for PCM and the fully bipolar operation needed for high-performance RRAM [1, 2].

These devices contain a large amount of mobile copper ions, which can move readily within the MIEC material. Our primary, ‘Process-Of-Record’ (POR) MIEC material is in fact more than 50% copper by weight. No silver (Ag)-based MIEC material has yet delivered similar IV characteristics when fabricated in a confined via. The discussion below considers a confined device fabricated from the Cu-containing POR material.

At low bias, Schottky barriers at the MIEC-electrode interfaces are believed to help suppress current flow, leading to the ultra-low leakage. As bias increases in either direction, copper ions and vacancies shift accordingly within the device, modulating the interfaces and leading to an exponential
increase in electronic current [6]. Although the current eventually saturates, extremely high current densities have been observed (up to 50 MA cm⁻² (figure 3) [1]).

The large amounts of copper present might suggest a filamentary role in the operation of these MIEC-based ADs, similar to the way CB-RAM [40] and even some memristive [41] NVM devices are known to operate. However, our extensive experimental evidence does not support this hypothesis at all. The turn-ON of symmetric MIEC-based ADs (figure 2(a)) does not exhibit filamentary behavior [2], and devices clearly show area-scaling of current over a wide range of electrode sizes (figure 3) [1]. The long-term repeatability and stability of MIEC-based ADs over a wide range of currents (figure 4) is also highly inconsistent with a filamentary role [5].

However, the I–V characteristics of highly asymmetric devices—such as the devices shown in (figure 2(b)) which have a top electrode contact (TEC) that is much larger (>80 μm diameter) than its bottom electrode contact (BEC) is much smaller (~30 nm) than the top electrode contact (>3 μm, ionizable TEC), are markedly different. Negative bias on the TEC produces very tight, exponential diode-like I–V characteristics. At moderate positive bias, Cu⁺ ions swept from the large TEC into the tiny via form a metallic filament, masking the diode-like action that would have been present in a symmetric device. Inset shows a dark-field TEM image of a device with the same nominal electrode dimensions, except that it used a non-ionizable (Tungsten) TEC—such devices exhibited similar I–V characteristics. (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [1, 2]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)

Figure 2. (a) Measured I–V characteristics for symmetric devices (here a 5 × 10 array of diode-in-via MIEC-based ADs, tested with integrated FETs) show an exponential increase of current for both polarities. The voltage margin, defined as the span over which median leakage remains below 10 nA, is tightly distributed (here Vₘₐₓ ∼ 1.1 V). (b) In contrast, superimposed I–V characteristics of sixty asymmetric devices, where the bottom electrode contact (BEC) is much smaller (~30 nm) than the top electrode contact (>3 μm, ionizable TEC), are markedly different. Negative bias on the TEC produces very tight, exponential diode-like I–V characteristics. At moderate positive bias, Cu⁺ ions swept from the large TEC into the tiny via form a metallic filament, masking the diode-like action that would have been present in a symmetric device. Inset shows a dark-field TEM image of a device with the same nominal electrode dimensions, except that it used a non-ionizable (Tungsten) TEC—such devices exhibited similar I–V characteristics. (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [1, 2]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)

Figure 3. Current in AD devices with ionizable, wide-area TECs scales perfectly with BEC area. Here 40 nm vias are defined in thinner (20 nm rather than 40 nm thick) dielectric to finesse limits of sputter deposition. Inset: ultrasmall (19 nm) AD with ionizable, wide-area TEC defined in thin (13 nm) dielectric passes currents > 165 μA (J > 50 MA cm⁻²). (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [1]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)
reduce cycling endurance. $\sim 10^9$ cycles has been demonstrated at $\sim 150 \mu A$ [2]. Endurance at lower currents is so high as to be difficult to measure, and is known to be $> 1 \times 10^{10}$ cycles at $\mu \sim 5 \mu A$ [1] and $> 12$ h of continuous dc exposure at $\sim 30 \mu A$ (figure 4(a)) [5].

While copper ions in a healthy symmetric MIEC-based AD are not able to form a filament, these ions do play a critical role in its electrical characteristics. Numerical simulations including both positively-charged copper ions as well as negatively-charged vacancy sites have been able to quantitatively match the electrical characteristics of MIEC-based ADs (figure 5) [6]. These simulations suggest that at low bias, mobile ions settle into a U-shaped distribution with large electric fields at each interface, maintaining a dynamic equilibrium between electrostatic ion drift towards, and ion diffusion away from, each interface. The strong ion accumulation at each interface results in residual electron tunneling at each interface, but strong suppression of holes and hole current. Device turn-ON occurs as hole injection from the positively-biased electrode increases sharply, driven by motion of large populations of copper ions and vacancies [6]. Asymmetry between top and bottom electrodes leads to asymmetric $I-V$ characteristics, since both ion densities and the mapping from current density to current are affected by the geometry of the device with respect to the polarity of operation.

Integration of MIEC-based ADs has been demonstrated on 8″ wafers, with Cu-containing MIEC material sputtered into vias followed by an optimized CMP process [2] and a confined, non-ionizable TEC. Conductive-AFM testing of short-loop devices with minimal wiring has validated single-target deposition and revealed a wide processing temperature window (up to 500°C) for these MIEC-based ADs [3]. Although these ADs do not need high processing temperatures, MIEC-based ADs would not be adversely affected if a co-integrated RRAM or other NVM did require such processing conditions.

Figure 4. MIEC-based ADs maintain (a) ultralow-leakage over hours of exposure, whether in a deep ($\pm 230$ mV) or shallow un-select ($\pm 350$ mV) condition, and even (b) repeated 2sec exposures to half-select ($\pm 530$ mV) and even higher bias conditions has minimal impact on subsequent leakage, all highly inconsistent with filamentary operation. (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [5]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)

Bi-directional array diagnostic monitor (ADM) arrays of up to 512 $\times$ 1024 integrated MIEC-based ADs have been tested using integrated 1-bit sense-amplifiers and a fast electrical tester (Magnum 2 EV) [3]. Cumulative distribution functions (CDFs) of the bitline voltage $V_{m}$ needed to produce various device currents $I_{d}$ show tightly distributed array $I-V$ characteristics (figure 6(a)). All 524 288 MIEC-based ADs—100% yield—had $V_{m} > 1.1$ V, and 99.955% of ADs fell within $\pm 150$ mV of the median voltage margin $V_{m} = 1.36$ V at 10 nA (figure 6(b)) [3]. Multiple such ADMs across two wafers showed very similar yield values.

Thickness scaling experiments showed that as MIEC-based ADs become thinner, voltage margin remains mostly
unchanged until the minimum gap between electrodes, \( d_{\text{min}} \), reaches \( \sim 11 - 12 \) nm [4]. Short-loop MIEC-based ADs fabricated with ultra-scaled vias show both high yield and high voltage margin [4]. Despite their small size, these MIEC-based ADs can still rapidly drive the large currents needed for NVM switching (figure 7(a)). Voltage margin \( V_m \) (at 10 nA) improves markedly as devices are scaled in lateral size. Aggressively-scaled short-loop MIEC-based ADs retain all requisite characteristics, including ultra-low leakage (<10 pA) and the large voltage margins (\( V_m > 1.50 \) V) needed for large arrays, even with both top and bottom critical dimensions (CDs) < 30 nm (figure 7(b), (c)). Unlike thickness scaling, where leakage increases sharply below \( d_{\text{min}} \sim 11 \) nm, no lower limit to CD scaling has yet been identified [4].

Integration of MIEC-based ADs immediately above small (CD \( \sim 35 \) nm) PCM devices allowed testing of integrated PCM+MIEC device pairs. Figure 8 demonstrates endurance in excess of 100,000 cycles, despite the repeated application of RESET pulses >200 \( \mu \)A and 5 \( \mu \)S long SET pulses at \( \sim 90 \mu \)A [3]. To demonstrate NVM write speed capabilities, an MIEC-based AD was used to rapidly RESET a co-integrated PCM device. After each 15 ns RESET pulse at varying amplitude (figure 9(a)), a long SET pulse recrystallized the doped-Ge\(_2\)Sb\(_2\)Te\(_5\) PCM material. After each pulse, bipolar dc \( I-V \) curves (figure 9(b), (c)) showed the expected change in the PCM resistance above the same low-leakage characteristics of the MIEC-based AD [4].

**Figure 6.** Cumulative distribution functions (CDFs) across bitline voltage \( V_{BL} \) at various device currents \( I_d \) (a) show array level \( I-V \) results with tight distributions across a 512 \( \times \) 1024 array of integrated MIEC-based ADs [3]. These devices were nominally the same lateral size as the device shown in the inset of figure 2(a), but were about 30% thinner. (b) Within this same 512 \( \times \) 1024 array, there were no leaky devices; 100% of the array showed \( V_m > 1.1 \) V, while 99.955% of MIEC-based ADs had voltage margins \( V_m \) at 10 nA within \( \pm 150 \) mV of the median of 1.36 V. (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [3]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)

**Figure 7.** (a) In addition to high yield, scaled short-loop MIEC-based ADs [4] exhibit the same \( > 1e7 \) ON-OFF contrast, < 50 ns turn-ON times (test-setup-limited), and ultra-low leakage shown in larger devices [2, 3]. Aggressively-scaled short-loop MIEC-based ADs, with (b) both TEC and BEC < 30 nm, also show (c) large voltage margins and ultra-low leakage. (Copyright c IEEE. All rights reserved. Reprinted, with permission, from [4]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)
Figure 8. Endurance of an integrated PCM+MIEC device-pair to > 100 k cycles, with RESET currents > 200 μA and 5 μs-long SET pulses (∼90 μA). No AD degradation or PCM failure had occurred at the time testing was terminated. (Copyright © IEEE. All rights reserved. Reprinted, with permission, from [3]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.)

Figure 9. After each (a) single 15 ns RESET pulse, bipolar dc I-V curves show the large resistance contrast (∼1 MΩ) of PCM RESET devices, yet the low-leakage characteristics of the MIEC-based AD remain unaffected, in both the (b) RESET and (c) SET states (Copyright © IEEE. All rights reserved. Reprinted, with permission, from [4]. Personal use of this material is permitted. However, permission to reuse this material for any other purpose must be obtained from the IEEE.).
We expect that MIEC-based ADs should prove equally compatible with integration of RRAM and STT-MRAM devices. For RRAM, the 180 nm test vehicle (ADM) used for figure 6 proved unsuitable, because it could not provide sufficient control over current compliance, either at the edge of the array or even at each device. Work is ongoing to integrate STT-MRAM devices together with MIEC ADs, but no test results are yet available. Challenges for STT-MRAM include rapid read and write speeds [5], as well as the need to distinguish between two very similar resistance states. These considerations—enforcing compliance and implementing low-contrast sensing—will be issues for any two-terminal AD, and not just for MIEC-based ADs. ADs that exhibit extremely low variability should provide a high degree of control over RRAM programming currents. However, initial research explorations will likely require reliable and independent control over compliance at each cell in order to unambiguously assess the performance of an RRAM integrated together with any two-terminal AD. Similarly, while low variability is essential for distinguishing low-contrast STT-MRAM read currents across a large array, the first step is to show that co-integration is viable and that single device-pairs can be switched and read reliably.

As mentioned previously, it has been shown that the ultra-low leakage offered by MIEC-based ADs representing the un-selected state can be held for hours (figure 4(a)), while higher half-selected leakage can be sustained for at least a few seconds (figure 4(b)), more than long enough for millions of successive 1μs reads to the same bitline [5]. In addition, MIEC-based ADs can return rapidly from either the selected-for-read or selected-for-write states [5]. The leakage recovery after write (30 – 50 μA) operations requires ~1 μs, with post-read (3 – 6 μA) recovery being even faster. The application of shaped pulses or a transient ‘overvoltage’ read readily allows MIEC-based ADs to support ~5–10 μA NVM reads in <50 ns, fast enough for use with MRAM (figure 10) [5].
Inherently-fast thin MIEC-based ADs offer similar speeds at modest overvoltages, which is important for minimizing the possibility of read disturb [5].

The design space for crossbar arrays composed of ADs based on MIEC has been explored using circuit-level SPICE simulations. This modeling shows that achievable array size and the excess required power during write depends strongly on careful matching between the turn-ON voltage \( V_{in} \) of the AD and the switching voltage \( V_{NVM} \) of the memory device (figure 11(a)) [7]. In contrast, the dependence of excess write power on NVM switching currents \( I_{NVM} \) is much less critical. Scaled MIEC-based devices (\( V_{in} \approx 1.54 \) V) have been shown to support arrays of 1 Mb in size up to NVM switching voltages of \( V_{NVM} \approx 1.2 \) V (figure 11(a)), and a simple stack of two MIEC-based devices enables \( V_{NVM} \approx 2.4 \) V (figure 11(b)) [7].

6. Conclusion

Access devices (ADs) based on copper-containing MIEC materials [1–7] make for an ideal companion to resistive-NVM devices for implementing large, densely-packed, multi-layer crossbar arrays. These MIEC-based ADs are well-suited for both the scaled CDs and thicknesses of advanced technology nodes, and for the fast read and write speeds of emerging NVM devices, and require only the low processing temperatures of the BEOL. They offer large currents (>100 \( \mu \)A), bipolar operation, large ON/OFF ratios (> 10\(^7\)), a significant voltage margin \( V_{in} \) (over which current < 10 nA), and ultra-low leakage (< 10 pA). Co-integration with PCM, integration in large (512 kBit) arrays with 100% yield and tight distributions, fast transient operation, long-term persistence of the required ultra-low-leakage, and scalability to aggressive technology nodes have all been demonstrated. The operation of these MIEC-based ADs is believed to depend on Cu-mediated hole conduction, and SPICE analysis has shown them to be highly suitable for any crossbar array built with resistive-NVM devices with modest (<2.5 V) switching voltages.

Future desired improvements in MIEC-based ADs would include better endurance at high current (currently \( \sim 10^8 \) cycles at 150 \( \mu \)A [2]), study of the temperature dependence of voltage margin, verification of high endurance and low variability in ultra-scaled devices at both high and low operating temperatures, and increases in the voltage margin so as to enable large arrays for NVM devices requiring larger switching voltages.

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