Jinho Lee

Curriculum Vitae

Researcher Staff Member
IBM Research
11501 Burnet, Austin, TX
Date of birth : 29 Sep., 1986
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leejinho@us.ibm.com

Research Interests

- Accelerators for big data processing
- Graph databases
- Near-data processing
- Human-robot interaction
- Other interests : Network-on-chips and memory system

Working Experience

2017 **Research Staff Member (Current),** *IBM Austin Research Lab,* Reseaching graph databases, accelerators and robotics.

2016-2017 **PostDoctoral Researcher,** *IBM Austin Research Lab,* Reseaching graph databases, accelerators and robotics.

2015 **Visiting Scholar,** *IBM Austin Research Lab,* Designing a cache coherent accelerator for graph processing.

Education

2011 – 2016 **Ph.D. Degree**, *Seoul National University*, South Korea.
Electrical Engineering and and Computer Science
Advisor: Prof. Kiyoung Choi
Thesis: "Designing Efficient On-chip Networks: Mapping, Management, and Routing"
Graduation: Feb, 2016
GPA: 4.02/4.30

2009 – 2011 **M.S. Degree**, *Seoul National University*, South Korea.
Electrical Engineering and Computer Science
Advisor: Prof. Kiyoung Choi
Thesis: "Memory-Aware Mapping of Tasks and Communications onto Many Core SoC"
GPA: 4.08/4.30

2005 – 2009 **B.S. Degree**, *Seoul National University*, South Korea.
Electrical Engineering
GPA: 3.98/4.30
Major GP: 4.08/4.30, Summa cum laude (the highest achievement in university)

Honors and Fellowship

2016 Best Thesis Award from EE, SNU

2016 HumanTech Paper Award - Bronze Award from Samsung Electronics

2011-2013 Global Ph.D. fellowship from National Research Foundation of Korea

2009-2011 Graduate student scholarship from Korea Foundation of Advanced Studies

2005-2009 National scholarship for science and engineering

2005 Top freshmen grand scholarship award from Seoul National University

Publications

Journal Publications

2017 **Jinho Lee**, Jongwook Chung, Jung Ho Ahn, and Kiyoung Choi. "Excavating the Hidden Parallelism Inside DRAM Architectures with Buffered Compares". In: *IEEE Transactions on VLSI* 25.6, pp. 1793–1806.

2017 **Jinho Lee**, Heesu Kim, Yoo Sungjoo, Kiyoung Choi, Gi-Joon Nam, H. Peter Hofstee, Mark Nutter, and Damir Jamsek. "ExtraV: Boosting Out-of-Memory Graph Processing with a Coherent Accelerator". In: *Proceedings of the VLDB Endowment* 10.12.

2017 Kyuseung Han, Woojoo Lee, Jaejin Lee, **Jinho Lee**, and Massoud Pedram. "TEI-NoC: Optimizing Ultra-Low Power NoCs Exploiting the Temperature Effect Inversion". In: *IEEE TCAD* (preprint).

2015 **Jinho Lee**, Kyungsu Kang, and Kiyoung Choi. "REDELF: An energy-efficient deadlock-free routing for 3-D NoCs with partial vertical connections". In: *ACM Journal of Emerging Technologies* 12.3, pp. 26:1–26:22.

2013 **Jinho Lee**, Moo-Kyoung Chung, Yeon-Gon Cho, Soojung Ryu, Jung Ho Ahn, and Kiyoung Choi. "Mapping and scheduling of tasks and communications on many-core soc under local memory constraint". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 32.11, pp. 1748–1761.

2013 **Jinho Lee**, Dongwoo Lee, Sunwook Kim, and Kiyoung Choi. "Deflection routing in 3D network-on-chip with limited vertical bandwidth". In: *ACM Transactions on Design Automation of Electronic Systems* 18.4, pp. 50:1–50:22.

Conference Publications

2017 D.Vijitbenjaronk, Warut, **Jinho Lee**, Toyotaro Suzumura, and Gabi Tanase. "Scalable Time-Versioning Support for Property Graph Databases". In: *Accepted to IEEE Bigdata*.

2017 Jian Fang, **Jinho Lee**, H. Peter Hofstee, and Jan Hidders. "Analyzing In-Memory Hash Joins: Granularity Matters". In: *International Workshop on Accelerating Analytics and Data Management Systems Using Modern Processor and Storage Architectures*.

2017 **Jinho Lee**, Inseok Hwang, Thomas Hubregtsen, Anne E. Gattiker, and Christopher M. Durham. "SCI-FII: Speculative conversational interface framework for incremental inference on modularized services". In: *International Conference on Mobile Data Management*.

2017 Tanase, Gabi, Toyotaro Suzumura, **Jinho Lee**, Chun-Fu (Richard) Chen, Jason Crawford, Hiroki Kanezashi, Song Zhang, and Warut D.Vijitbenjaronk. "System G Distributed Graph Database". In: *Submitted to ICDE*.

2016 **Jinho Lee**, Jung Ho Ahn, and Kiyoung Choi. "Buffered compares: Excavating the hidden parallelism inside DRAM architectures with lightweight logic". In: *Design, Automation and Test in Europe (Best paper candidate)*, pp. 1243–1248.

2015 **Jinho Lee**, Junwhan Ahn, Kiyoung Choi, and Kyungsu Kang. "THOR: Orchestrated thermal management of cores and networks in 3D many-core architectures". In: *Asia and South Pacific Design Automation Conference*, pp. 773–778.

2014 Sungju Han, **Jinho Lee**, and Kiyoung Choi. "Tree-mesh heterogeneous topology for low-latency NoC". In: *International Workshop on Network on Chip Architectures*, pp. 19–24.

2013 Gunhee Lee, **Jinho Lee**, and Kiyoung Choi. "Towards optimal adaptive routing in 3D NoC with limited vertical bandwidth". In: *International Workshop on Network on Chip Architectures*, pp. 23–26.

2013 **Jinho Lee** and Kiyoung Choi. "A deadlock-free routing algorithm requiring no virtual channel on 3D-NoCs with partial vertical connections". In: *International Symposium on Networks-on-Chip*, pp. 1–2.

2013 **Jinho Lee**, Dongwoo Lee, Sunwook Kim, and Kiyoung Choi. "Deflection routing in 3D network-on-chip with TSV serialization". In: *Asia and South Pacific Design Automation Conference*, pp. 29–34.

2012 **Jinho Lee** and Kiyoung Choi. "Memory-aware mapping and scheduling of tasks and communications on many-core SoC". In: *Asia and South Pacific Design Automation Conference*, pp. 419–424.

2012 Mingyang Zhu, **Jinho Lee**, and Kiyoung Choi. "An adaptive routing algorithm for 3D mesh NoC with limited vertical bandwidth". In: *International Conference on VLSI and System-on-Chip*, pp. 18–23.

2011 **Jinho Lee**, Mingyang Zhu, Kiyoung Choi, Jung Ho Ahn, and Rohit Sharma. "3D network-on-chip with wireless links through inductive coupling". In: *International SoC Design Conference*, pp. 353–356.

2009 Hanmin Park, Jong Kyung Paek, **Jinho Lee**, and Kiyoung Choi. "Leakage power reduction of functional units in processors having zero-overhead loop counter". In: *International SoC Design Conference*, pp. 492–495.

Patents

2016 **Jinho Lee**, Moo-kyoung Chung, KiYoung Choi, Yeon-gon Cho, and Soo-jung Ryu. *Method of compiling program to be executed on multi-core processor, and task mapping method and task scheduling method of reconfigurable processor*. US Patent 9,298,430.

Research Experience

2015 **Accelerator design using IBM CAPI**, *Project leader*.
Developing an accelerator for large graph-processing with coherent bus architecture.

2016 **Graph database**, *Researcher*.
Graph database that supports time-versioned features with KV store.

2016 **Human-robot interaction**, *Researcher*.
Developing a robot conversation system for customer-service.

2013–2015 **Designing a many-core architecture**, *Project leader*.
Project management, developing architectural specifications including memory system and interconnection network. Developing a simulator for design space exploration

2012–2013 **Developing a coherency cache system**, *Team leader*.
Designing a cache coherence protocol, developing simulators for NoC and cache system, developing RTL codes for cache system

2013–2016 **Near data processing**, *Project Leader*.
Efficient memory architecture for near data processing

2009–2013 **Desigining a 3D NoC**, *Researcher*.
Research topics on NoC includes mapping applications to 3D NoC, routing algorithms, and thermal management techniques

Reviews

2014 **Computers & Electrical Engineering,** *Elsevier,* Served as a reviewer for two papers.

2015 **Microprocessors and Microsystems,** *Elsevier,* Served as a reviewer for a paper.

2015 **Transactions on Computer-Aided Design of Integrated Circuits and Systems,** *IEEE,* Served as a reviewer for a paper.

2016 **Computer Architecture Letter,** *IEEE,* Served as a reviewer for a paper.

2016 **DAC PhD forum,** Served as a reviewer for four papers.

2016 **Design Automation for Embedded Systems,** *Springer,* Served as a reviewer for a paper.

2016 **Design & Test,** *IEEE,* Served as a reviewer for a paper.

2016 **Microelectronics Journal,** *Elsevier,* Served as a reviewer for two papers.

2017 **The Computer Journal,** *Elsevier,* Served as a reviewer for a paper.

2017 **International Parallel & Distributed Processing Symposium,** *IEEE,* Served as a reviewer for a paper.

2017 **Transactions on Embedded Computing Systems,** *ACM,* Served as a reviewer for a paper.

2017 **Design & Test,** *IEEE,* Served as a reviewer for two papers.

2017 **Transactions on Computer,** *IEEE,* Served as a reviewer for a paper.

2017 **Transactions on VLSI,** *IEEE,* Served as a reviewer for a paper.

2017 **Frontiers of Information Technology & Electronic Engineering,** *Springer,* Served as a reviewer for a paper.

2017 **Journal of Low Power Electronics,** *ASP,* Served as a reviewer for a paper.

Skills

Languages C, C++, Java, Python, Ruby, Assembly

HDL Verilog, VHDL

Simulators Architecture: gem5, Sniper, McsimA+, Soc Designer, etc
Power/Thermal: McPAT, Hotspot
Hardware: Modelsim, VCS

Others FPGA (Xilinx, Altera), SPICE, MATLAB

Memberships

IEEE Member

ACM Member

Languages

English **Fluent** *All work performed in English*

Korean **Native** *Mother Tongue*

Working/Teaching Experience

2013 **Teaching Assistant,** *SoC Design Automation,* Independently led three lectures, supervised lab classes and graded homeworks, tests and projects

2012 **Teaching Assistant,** *Digital Logic Design,* Supervised lab classes and graded homeworks, tests and projects

2011 **Teaching Assistant,** *Introduction to Computers,* Supervised lab classes and graded homeworks, tests and projects

Personal Pages

Personal profile `http://researcher.watson.ibm.com/researcher/view.php?person=us-leejinho`

Google scholar `https://scholar.google.com/citations?hl=ko&user=pm3Fso0AAAAJ&view_op=list_works`

Linkedin `https://www.linkedin.com/in/jinho-lee-a2987274/`