Transmitter Predistortion for Simultaneous Improvements in Bit Rate, Sensitivity, Jitter, and Power Efficiency in 20 Gb/s CMOS-Driven VCSEL Links

Abstract—The effect of applying feed-forward equalization (FFE) on the transmitter side is studied for three different full optical links. In contrast to all previous works, the FFE settings are optimized for a complete link, rather than just the vertical-cavity surface-emitting laser output. The approach results in dramatic improvements in total link performance: >6 dB in sensitivity, 3X in timing margin, and 2X in power efficiency at 15 Gb/s, and a record 5.7 pJ/bit at 20 Gb/s.

Index Terms—CMOS analog integrated circuits, driver circuits, equalization, feed-forward equalization (FFE), optical communication, optical receivers, optoelectronic devices, photodetectors, photodiodes (PDs), pre-emphasis, semiconductor lasers.

I. INTRODUCTION

MULTIMODE vertical-cavity surface-emitting laser (VCSEL) transceivers dominate the short-reach optical market, from serial Ethernet and Fiber-channel transceivers to parallel transceivers and active optical cables for high-performance computing and switch/routers. VCSEL-based interconnects offer many advantages including 1) low device fabrication cost with wafer-scale burn-in and testing, 2) inexpensive assembly utilizing injection molded plastic optical systems with wide alignment tolerances, and 3) simple driver design due to low VCSEL thresholds and reasonable impedances. However, as data rates move to 20 Gb/s and higher, challenges emerge. Single VCSELs have been demonstrated at 30–40 Gb/s at several wavelengths [1], [2], but yielding adequate bandwidth in a reliable production device may prove difficult. One of the most arduous challenges to achieving high data rates in multimode links is the receivers. High data rates are more easily achieved with small photodiodes (PDs), but as devices shrink, assembly costs rise as alignment tolerances tighten. Achieving sufficient receiver bandwidth through the receiver (RX) front-end and limiting amplifier (LA) will be challenging, especially for CMOS designs optimized for power efficiency and compatibility with reasonably sized PDs (25–40 μm diameter).

Unlike a typical short-reach electrical link (backplane or chip-to-chip), the multimode fiber (MMF) is not introducing excessive amounts of loss or dispersion, even over distance scales on the order of a hundred meters. As a result, short-reach optical interconnects feature nearly ideal channel performance with little or no need for equalization. From the purely electrical point of view, however, the full end-to-end communication channel is not limited to the MMF alone. Electrical data need to be converted into an optical form, received, and amplified. It is natural, therefore, to broaden the definition of the “channel” to include the VCSEL, the PD and the RX front end, as illustrated in Fig. 1. When one considers this broadly defined channel at speeds of 20 Gb/s and above, its characteristics are far from ideal and communication over this channel can definitely benefit from equalization.

Feed-forward equalization (FFE) of VCSEL-based optical transmitters is a well-known technique [3]–[14]. All previously reported results, however, have not utilized the full power of equalization, focusing exclusively on boosting the VCSEL bandwidth. It is important to note that for high-speed operation, the VCSEL is typically biased well into the linear mode of operation (far above threshold). The application of the FFE-shaped transmit signal through the VCSEL can, therefore, be used to speed up both the transmitter (TX) and the receiver, improving the overall link performance.

Fig. 1. Optical link block diagram. The definition of the communication channel is generalized to include VCSEL, MMF, PD, and the RX front end.
In this paper, we study the effect of TX FFE for three different receivers, observing significant improvements in the overall performance for all three optical links. The TX FFE is tunable in a wide range and the settings are independently optimized for each full link, targeting the total end-to-end link performance metrics. The corresponding VCSEL optical outputs are recorded, but only to document the internal signals in the channel. At channel-optimized TX FFE settings the VCSEL optical output might be overequalized and appear to be deviating from the optimum point. But the final electrical data on the RX side show a significant benefit from the predistorted optical waveform generated by the TX. Application of TX FFE to the full link produces results that are hard or impossible to obtain by optimizing the VCSEL output alone.

This paper is organized as follows. After a brief introduction, we start with overview of VCSEL equalization techniques in Section II. Section III describes the FFE-enabled VCSEL driver used in all experiments. Sections IV, V, and VI present the three different receivers, with results for all three corresponding full optical links. The results are summarized in the conclusion in Section VII.

II. OVERVIEW OF VCSEL EQUALIZATION TECHNIQUES

A number of methods for shaping the driver current waveform in order to speedup the VCSEL optical response have been reported in the literature [3]–[14]. Several relatively complicated equalization schemes have been proposed to exactly cancel VCSEL dynamics [3], [4]. Although interesting from theoretical point of view, the desired current waveforms are hard to implement, especially at high data rates. For many practical purposes, however, VCSEL can be modeled as a low-pass filter, so a natural equalization technique would be to create a driver with a high-pass characteristic [5]–[7]. The combined driver-plus-VCSEL system would then become more broadband, enabling data transfer at data rates well above the VCSEL bandwidth. A peaked current waveform can be created by simply adding a speedup inductor to the driver [8], [9]. While this approach was shown to work, it has a number of disadvantages. It introduces a significant area overhead, but, most importantly, the parameters of the inductor-based high-pass filter are not tunable, making it harder to exactly match the VCSEL characteristic. In a digital system, the high-pass driver can be realized with a latch-based FFE [10]. One advantage of a digital FFE is that the filter tap spacing automatically tracks the bit interval. This feature, however, is only important for filters with a large number of taps. The power and area overheads associated with clock distribution and latching of high-speed data make a digital FFE system far less attractive than a continuous-time FFE [7], [11], where the delay between the filter taps is created by a tunable delay line.

Regardless of the particular equalization scheme, all previously reported results focused on using FFE for optimizing the optical output of the VCSEL. Some equalization efforts [12], [13] specifically addressed the raise/fall time asymmetry of the VCSEL and [14] additionally included equalization of modal dispersion in a long MMF link. None of these works studied the benefits of transmitter-side equalization on a full optical link.

III. FFE-ENABLED TRANSMITTER

The block diagram of the VCSEL driver with one-tap continuous-time FFE is shown in Fig. 2. This is the transmitter that was used in all full-link experiments described in this paper. The driver consists of a five-stage Cherry–Hooper preamplifier (PA) followed by a current-mode logic (CML) output stage that implements the feed-forward equalizer. The FFE is powered by a single supply, VDD_OS, and operates by tapping a portion of the PA output signal, delaying and buffering it, then subtracting it from the main portion of the PA signal (graphically shown in Fig. 2). Note that although not explicitly shown in Fig. 2, the transmitter is a fully differential design. Fig. 2 also includes a graphical illustration of the FFE circuit operation. The height of the equalization pulse, represented by an overshoot or undershoot at each data transition edge, is controlled by tap weight (via vb_tab). The width of the equalization pulse is controlled by the delay (via vb_delay). The preemphasis can be completely turned off by grounding the vb_tab and vb_delay pins.

The transmitter and all three receiver circuits reported in this paper were fabricated in standard bulk digital 90 nm CMOS (IBM’s CMOS9SF process). The micrograph of the TX chip is shown in Fig. 3 together with the measured electrical eye diagrams at 10 and 20 Gb/s with FFE enabled. The fully assembled FFE TX is shown in Fig. 4.

The wirebond test site includes two 5 μm diameter VCSELs to balance the load on the output stage. Only one VCSEL was used in the full-link experiments described below. Also shown in Fig. 4 are the decoupling capacitors for each of the power supplies used in the experiment and an interposer for landing the high-speed probes. The interposer was used to improve the
mechanical robustness of the test site and the electrical reproducibility of the measurements.

IV. TRANSMITTER EQUALIZED FULL LINK WITH RECEIVER 1

TX and RX assemblies were made by attaching CMOS chips to test cards and wire bonding all power, ground and bias connections. Short wire bonds were used to connect the VCSELs and PDs to their respective ICs. All high-speed electrical I/O was applied and collected using coplanar GSGSG microwave probes, while lensed 50 μm MMF probes were used for both the TX and RX optical coupling. A 30 GHz bandwidth sampling oscilloscope was used for all eye-diagram measurements, and a 17 GHz bandwidth Newport D-25xr PD was employed for transmitter eye-diagrams. The pattern was 2^7 – 1 PRBS and the signal applied at the FFE TX input was 500 mVp-p.

The VCSEL and PD arrays for all of the links presented here were designed and fabricated by Emcore Corporation. Both of the devices are conventional 850 nm top-emitting/detecting mesa structures fabricated on un-thinned semi-insulating substrates using a volume production process. Further details of the VCSEL and PD growth and fabrication can be found in [15]. The VCSEL in the FFE transmitter had an aperture of 5 μm, a series resistance of approximately 50 Ω, and a slope efficiency of ~0.4 mW/mA. All of the receivers utilized 25 μm diameter devices with a responsivity of 0.55 A/W, and a capacitance of 76 fF at their nominal—3 V bias point.

A block diagram of the full link containing the CMOS receiver that will be referred to as RX1 is shown in Fig. 5. The RX1 receiver is the first design we implemented in 90 nm CMOS [9] and its bandwidth was lower than expected. Although this receiver did operate up to 20 Gb/s when tested with a high-speed reference VCSEL, it did not support full CMOS links at 15–20 Gb/s with transmitters constructed with first-generation 90 nm CMOS laser drivers. The RX1 design was a fully differential transimpedance amplifier (TIA) followed by a five-stage Cherry–Hooper LA, two CML buffer stages and a final differential output driver. The TIA is ac coupled through on-chip capacitors nominally valued at 2.5 pF. The low-frequency cutoff of the receiver, including the front-end ac coupling and the active offset compensation loop surrounding the LA, is <50 MHz, sufficient to minimize the power penalty due to baseline wander assuming balanced 8b/10b data encoding. Device-level schematics for the RX1 chip can be found in [16]. Power supplies were separated for the TIA, LA, and output buffers to minimize both power consumption and switching-induced power supply noise.

Fig. 6 presents the TX output and RX electrical output eye diagrams measured for the RX1 link at data rates from 15 to 20 Gb/s with and without TX predistortion. Although only explicitly shown on the 15 Gb/s eye diagrams, the vertical scales are the same at the other data rates.

The link total power dissipation was therefore 165 mW with, and 160 mW without predistortion. As Fig. 6 illustrates, the effect of transmitter predistortion is dramatic. While the TX eye diagrams are visibly distorted when the FFE circuit is operating, the quality of the RX electrical output is improved at all data rates with reduced jitter and wide-open eye diagrams at 17.5 and 20 Gb/s.

The visible improvements in eye-diagram quality affected by TX predistortion translate into better sensitivity and timing.
margin. Fig. 7 presents the receiver sensitivity characteristics for the RX1 link as a function of data rate with and without TX predistortion. The RX sensitivity is improved by >7 dB at 15 Gb/s. With the TX FFE enabled, the link is operational at 20 Gb/s, whereas without equalization the link is limited to data rates <15 Gb/s. With TX predistortion, the receiver sensitivity at 20 Gb/s at a bit error ratio (BER) of $10^{-12}$ is $-8$ dBm and improves to better than $-15$ dBm at 10 Gb/s.

The timing margin characteristics for the RX1 link are shown in Fig. 8 at a data rate of 15 Gb/s. TX predistortion improves the horizontal eye opening at BER = $10^{-11}$ by 0.22 unit interval (UI), or 28 ps, at 15 Gb/s. With TX predistortion, the timing margin (at BER = $10^{-11}$) is 0.24 UI (12 ps) at 20 Gb/s and 0.78 UI (78 ps) at 10 Gb/s.

It is instructive to plot the power efficiency of optical links as a function of data rate. Fig. 9 presents the power efficiency of the RX1 link when operated with and without TX predistortion for speeds up to 20 Gb/s. The curve in Fig. 9 was obtained as follows. At a given data rate, the best power efficiency was obtained by minimizing the link power consumption while ensuring that two conditions were satisfied: 1) the BER remained less than $10^{-12}$; and 2) the RX output voltage swing was greater than 200 mV p-p. In general, an optical link will have an optimum data rate at which it operates most efficiently. At this optimum speed, the link is gain limited, i.e., the link is operating at a very low error rate and the power consumption is determined by meeting the second criteria of a minimum RX output voltage swing. Above the optimum rate, the extra power (mW) required to maintain performance typically outpaces the increased data rate (Gb/s), degrading the efficiency in mW/Gb/s, or equivalently, pJ/bit. At low data rates, the power efficiency curve also rises: since the link is operating at its gain-limited minimum power, the efficiency degrades as the data rate is lowered because the link power dissipation is amortized over fewer transferred bits. The power efficiency curve without TX predistortion clearly exhibits an optimum data rate, but the curve with predistortion is flattened. Between 10 and 17.5 Gb/s, the equalized RX1 link operates at a power efficiency of slightly less than 6 pJ/bit. At 20 Gb/s, the power efficiency of the equalized RX1 link is 8.3 pJ/bit.

V. TRANSMITTER EQUALIZED FULL LINK WITH RECEIVER 2
The block diagram of the second optical link, using a CMOS receiver that will be referred to here as the RX2 design, is shown in Fig. 10. The RX2 chip is a second-generation chip that was targeted specifically at achieving higher bandwidth than the original RX1 circuit. Consequently, there are substantial differences between the RX1 and RX2 designs. The RX2 LA was implemented with only Cherry–Hooper stages, eliminating the CML stages in the output block of the RX1 chip. An additional stage was added to the LA, bringing the total to six, to compensate for the reduced gain incurred by removing the CML stages. The LA in the RX2 design directly drives an inductively peaked differential output stage. Finally, although the differential TIA architecture was unchanged between the RX1 and RX2 circuits, the value of the transimpedance resistors were reduced by a factor of 2 in the RX2 design in an effort to improve the speed and, therefore, sensitivity at higher data rates, at the expense of reduced sensitivity at lower data rates.

Testing of the RX2 link proceeded in the same manner described previously for the RX1 link. Single-ended electrical
output eye diagrams produced by the RX2 link under multiple operating conditions as a function of data rate are presented in Fig. 11. Fig. 11(a) shows data for the link operating with no TX predistortion; the eye diagram at 17.5 Gb/s is starting to close and is completely closed at 20 Gb/s. Fig. 11(b) and (c) was obtained on the RX2 link with TX predistortion at two different receiver operating points. The data in Fig. 11(a) and (b) were obtained with the RX2 receiver consuming 85 mW, while in Fig. 11(c), the RX2 operated at a lower power dissipation of 53 mW. The FFE TX was set to the same conditions as in Fig. 5(a) and (b) so the TX eye diagrams are not repeated here. As with the RX1 link, TX predistortion yields visible improvements to the total link performance and extends the operating range of the link to 20 Gb/s.

The receiver sensitivity characteristics of the RX2 link are shown in Fig. 12 for the same operating conditions used to obtain the eye diagrams of Fig. 11. The curves in Fig. 12(a) were taken with no TX predistortion at a receiver power dissipation of 85 mW, the data in (b) were obtained at the same RX setting but with TX predistortion enabled, and the characteristics in (c) were obtained at the lower RX power dissipation setting of 53 mW. Directly comparing Fig. 12(a) and (b), it is evident that under the same RX operating conditions, TX predistortion improves the sensitivity at $\text{BER} = 10^{-12}$ by more than 4 dB at 15 Gb/s and extends the capability of the link to 20 Gb/s.

Fig. 13 plots the timing margin for the RX2 link with and without TX predistortion at the 85 mW RX power setting. At 15 Gb/s and $\text{BER} = 10^{-11}$, predistortion yields an improvement of 0.09 UI (6 ps). Comparing the 17.5 Gb/s data illustrates a much larger improvement with TX predistortion: without it, the link does not operate below $\text{BER} = 10^{-9}$, while with predistortion, the link has a 0.46 UI (31 ps) horizontal eye opening at $\text{BER} = 10^{-11}$. At 20 Gb/s, with TX predistortion, the timing margin is 0.42 UI (28 ps) at $\text{BER} = 10^{-11}$.

The power efficiency of the RX2 link as a function of data rate was measured in the same manner as described previously for the RX1 link and the results are plotted in Fig. 15. As with the RX1 link, the power efficiency curve as a function of data rate is significantly flattened with TX pre-distortion. The RX2
Fig. 14. Sensitivity and timing margin data for the RX2 link operating with TX predistortion through up to 150 m of OM4 fiber. (a) Receiver sensitivity characteristics at 17.5 Gb/s. (b) Timing margin at 17.5 Gb/s. (c) Timing margin at 20 Gb/s. The RX2 chip power consumption was 85 mW for all the datasets.

Fig. 15. Power efficiency as a function of data rate for the RX2 link with and without TX predistortion.

Fig. 16. Block diagram of the double-equalized full link incorporating the RX3 receiver.

The RX2 link achieves its best power efficiency of 4.6 pJ/bit at 15 Gb/s, and at 20 Gb/s the power efficiency is 5.7 pJ/bit. These numbers are the best efficiencies reported to date for a complete optical link operating at a data rate > 10 Gb/s.

VI. DOUBLE EQUALIZED FULL LINK WITH RECEIVER 3

The last link we report here is shown in Fig. 16 and incorporates a receiver chip that will be referred to as RX3. As with the RX2 circuit, RX3 is a second generation design. Both RX2 and RX3 share the same differential TIA and use the same Cherry–Hooper stages in the LA. However, the RX3 chip only uses five Cherry–Hooper LA stages. Following the LA is an FFE circuit similar to the equalizer in the TX chip that was described in Section III.

The FFE output driver in the RX3 chip was specifically designed to improve signal integrity when driving through lossy package and printed circuit board (PCB) interconnects. In order to illustrate the capabilities of the RX3 chip, one of its outputs was connected through a 10" PCB trace on a Nelco 4000 PCB as shown in Fig. 17. In this configuration, there are two links: the optical link between the TX and RX and the electrical link through the PCB between the RX output and the test equipment. In the data that follow, the total link power dissipation was 206 mW.

Fig. 18 presents eye diagrams at 20 Gb/s taken at the TX output, the directly probed RX output, and the RX output that traverses 10" of PCB trace, for two link conditions: double equalized with both TX and RX FFE circuits enabled, and with no equalization.

Fig. 19. Receiver sensitivity characteristics for the RX3 link (a) at 15 Gb/s with TX and RX equalization enabled, with only TX equalization and with only RX equalization, and (b) at 10, 12.5, 15, 17.5, and 20 Gb/s with both TX and RX FFE circuits enabled.
equalizers is dramatically illustrated by Fig. 18. Without equalization the link is broken, even at the directly probed RX output. With both TX and RX equalization enabled, the link is operational even with the extra 10⁷ PCB trace included.

Fig. 19 presents receiver sensitivity characteristics for the RX3 link. Fig. 19(a) plots the RX sensitivity at 15 Gb/s measured after the 10⁷ PCB trace under three different conditions: double equalization, transmitter equalization without receiver equalization, and receiver equalization without transmitter equalization. At 15 Gb/s, both TX and RX equalization is required to successfully close the optical and PCB electrical links. Fig. 19(b) plots the RX3 sensitivity characteristics measured after the PCB trace at multiple data rates up to 20 Gb/s.

VII. CONCLUSION

The effect of transmitter equalization is studied for three VCSEL-based multimode optical links. Unlike all previous works, the TX FFE settings are optimized for the entire link, including the receiver. Wide tuning range of the TX FFE allows strong predistortion of the VCSEL output, resulting in a dramatic improvement of all key metrics of the overall link performance. The example of the bandwidth-limited receiver RX1 described in Section IV is particularly striking: a link that struggled at 15 Gb/s was made to operate at 20 Gb/s. At 15 Gb/s, transmitter predistortion was shown to improve the sensitivity by >7 dB, horizontal eye opening by 3X, and the overall link efficiency by 2X. The demonstrated performance gains can be used to reliably build high-speed links using slower components, for example, receivers incorporating larger PDs.

We believe that the technique of transmitter pre-distortion demonstrated here offers a path to better performance and operating margin at all data rates and will be a powerful tool in extending the dominance of VCSEL-based interconnects for short-reach applications to data rates beyond 25 Gb/s.

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REFERENCES

[1] [Please provide the names of all the authors in Refs. [1] and [7]–[16].]


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In 1999, he joined IBM in Rochester, MN, assuming responsibility for the optical receivers used in IBM’s optical transceiver business. From 2001 to 2004, he was with Agility Communications in Santa Barbara, CA, developing high-speed optoelectronic modulators and tunable laser sources for optical communications. In 2004, he joined the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member. He is the author or coauthor of more than 100 journal or conference articles. He has six issued and more than ten pending patents. His current research interests include parallel optical interconnect technologies and high-speed CMOS circuits for fiber-optic data links.

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In 2009, he joined IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he is currently a Research Staff Member. He is also an Assistant Adjunct Professor of electrical engineering at Columbia University, New York. His research interests include silicon photonic devices, integrated optical switches and networks for high-performance computing systems and datacenters, and highly parallel multimode transceivers.

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He joined IBM Research in 1981, initially studying femtosecond electron and exciton dynamics in semiconductors. In 1995, he invented picosecond imaging circuit analysis, an optical technique which is used today to debug advanced CMOS ICs. From 2000 to 2011, he was focused on the use of optical interconnects in next and future generations of supercomputers, directing DARPA-sponsored IBM programs for chip-to-chip optical interconnects and nanophotonic optical switches. In 2011, he moved to Columbia University, New York, where he continues to direct research programs in optics. He has published more than 150 papers in major technical journals and holds 23 patents.

Dr. Kash is a Fellow of the American Physical Society. He also serves as a member of the IEEE Photonics Society Board of Governors and is also the Vice President for Membership.
Transmitter Predistortion for Simultaneous Improvements in Bit Rate, Sensitivity, Jitter, and Power Efficiency in 20 Gb/s CMOS-Driven VCSEL Links

Alexander V. Rylyakov, Clint L. Schow, Senior Member, IEEE, Benjamin G. Lee, Member, IEEE, Fuad E. Doany, Christian Baks, and Jeffrey A. Kash, Fellow, IEEE

Abstract—The effect of applying feed-forward equalization (FFE) on the transmitter side is studied for three different full optical links. In contrast to all previous works, the FFE settings are optimized for a complete link, rather than just the vertical-cavity surface-emitting laser output. The approach results in dramatic improvements in total link performance: >6 dB in sensitivity, 3X in timing margin, and 2X in power efficiency at 15 Gb/s, and a record 5.7 pJ/bit at 20 Gb/s.

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[Please check whether the affiliations of the authors are OK as typeset.] Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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In this paper, we study the effect of TX FFE for three different receivers, observing significant improvements in the overall performance for all three optical links. The TX FFE is tunable in a wide range and the settings are independently optimized for each full link, targeting the total end-to-end link performance metrics. The corresponding VCSEL optical outputs are recorded, but only to document the internal signals in the channel. At channel-optimized TX FFE settings the VCSEL optical output might be overequalized and appear to be deviating from the optimum point. But the final electrical data on the RX side show a significant benefit from the predistorted optical waveform generated by the TX. Application of TX FFE to the full link produces results that are hard or impossible to obtain by optimizing the VCSEL output alone.

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mechanical robustness of the test site and the electrical reproducibility of the measurements.

IV. TRANSMITTER EQUALIZED FULL LINK WITH RECEIVER 1

TX and RX assemblies were made by attaching CMOS chips to test cards and wire bonding all power, ground and bias connections. Short wire bonds were used to connect the VCSELs and PDs to their respective ICs. All high-speed electrical I/O was applied and collected using coplanar GSGSG microwave probes, while lensed 50 µm MMF probes were used for both the TX and RX optical coupling. A 30 GHz bandwidth sampling oscilloscope was used for all eye-diagram measurements, and a 17 GHz bandwidth Newport D-25xr PD was employed for transmitter eye-diagrams. The pattern was $2^7 - 1$ PRBS and the signal applied at the FFE TX input was 500 mVpp.

The VCSEL and PD arrays for all of the links presented here were designed and fabricated by Emcore Corporation. Both of the devices are conventional 850 nm top-emitting/detecting mesa structures fabricated on un-thinned semi-insulating substrates using a volume production process. Further details of the VCSEL and PD growth and fabrication can be found in [15]. The VCSEL in the FFE transmitter had an aperture of 5 µm, a series resistance of approximately 50 Ω, and a slope efficiency of ~0.4 mW/mA. All of the receivers utilized 25 µm diameter devices with a responsivity of 0.55 A/W, and a capacitance of 76 fF at their nominal—3 V bias point.

A block diagram of the full link containing the CMOS receiver that will be referred to as RX1 is shown in Fig. 5. The RX1 receiver is the first design we implemented in 90 nm CMOS [9] and its bandwidth was lower than expected. Although this receiver did operate up to 20 Gb/s when tested with a high-speed reference VCSEL, it did not support full CMOS links at 15–20 Gb/s with transmitters constructed with first-generation 90 nm CMOS laser drivers. The RX1 design was a fully differential transimpedance amplifier (TIA) followed by a five-stage Cherry–Hooper LA, two CML buffer stages and a final differential output driver. The TIA is ac coupled through on-chip capacitors nominally valued at 2.5 pF. The low-frequency cutoff of the receiver, including the front-end ac coupling and the active offset compensation loop surrounding the LA, is <50 MHz, sufficient to minimize the power penalty due to baseline wander assuming balanced 8b/10b data encoding. Device-level schematics for the RX1 chip can be found in [16]. Power supplies were separated for the TIA, LA, and output buffers to minimize both power consumption and switching-induced power supply noise.

Fig. 6 presents the TX output and RX electrical output eye diagrams measured for the RX1 link at data rates from 15 to 20 Gb/s with and without TX predistortion. Although only explicitly shown on the 15 Gb/s eye diagrams, the vertical scales are the same at the other data rates. The link total power dissipation was therefore 165 mW with, and 160 mW without predistortion. As Fig. 6 illustrates, the effect of transmitter predistortion is dramatic. While the TX eye diagrams are visibly distorted when the FFE circuit is operating, the quality of the RX electrical output is improved at all data rates with reduced jitter and wide-open eye diagrams at 17.5 and 20 Gb/s.

The visible improvements in eye-diagram quality affected by TX predistortion translate into better sensitivity and timing
Fig. 7. Receiver sensitivity characteristics for the RX1 link at multiple data rates (a) without and (b) with TX predistortion.

Fig. 8. Timing margin characteristics for the RX1 link at 15 Gb/s (a) without and (b) with TX predistortion.

margin. Fig. 7 presents the receiver sensitivity characteristics for the RX1 link as a function of data rate with and without TX predistortion. The RX sensitivity is improved by >7 dB at 15 Gb/s. With the TX FFE enabled, the link is operational at 20 Gb/s, whereas without equalization the link is limited to data rates <15 Gb/s. With TX predistortion, the receiver sensitivity at 20 Gb/s at a bit error ratio (BER) of 10^{-12} is ~8 dBm and improves to better than ~15 dBm at 10 Gb/s.

The timing margin characteristics for the RX1 link are shown in Fig. 8 at a data rate of 15 Gb/s. TX predistortion improves the horizontal eye opening at BER = 10^{-11} by 0.42 unit interval (UI), or 28 ps, at 15 Gb/s. With TX predistortion, the timing margin (at BER = 10^{-11}) is 0.24 UI (12 ps) at 20 Gb/s and 0.78 UI (78 ps) at 10 Gb/s.

It is instructive to plot the power efficiency of optical links as a function of data rate. Fig. 9 presents the power efficiency of the RX1 link when operated with and without TX predistortion for speeds up to 20 Gb/s. The curve in Fig. 9 was obtained as follows. At a given data rate, the best power efficiency was obtained by minimizing the link power consumption while ensuring that two conditions were satisfied: 1) the BER remained less than 10^{-12}; and 2) the RX output voltage swing was greater than 200 mV ppk. In general, an optical link will have an optimum data rate at which it operates most efficiently. At this optimum speed, the link is gain limited, i.e., the link is operating at a very low error rate and the power consumption is determined by meeting the second criteria of a minimum RX output voltage swing. Above the optimum rate, the extra power (mW) required to maintain performance typically outpaces the increased data rate (Gb/s), degrading the efficiency in mW/Gb/s, or equivalently, pJ/bit. At low data rates, the power efficiency curve also rises: since the link is operating at its gain-limited minimum power, the efficiency degrades as the data rate is lowered because the link power dissipation is amortized over fewer transferred bits. The power efficiency curve without TX predistortion clearly exhibits an optimum data rate, but the curve with predistortion is flattened. Between 10 and 17.5 Gb/s, the equalized RX1 link operates at a power efficiency of slightly less than 6 pJ/bit. At 20 Gb/s, the power efficiency of the equalized RX1 link is 8.3 pJ/bit.

V. TRANSMITTER EQUALIZED FULL LINK WITH RECEIVER 2

The block diagram of the second optical link, using a CMOS receiver that will be referred to here as the RX2 design, is shown in Fig. 10. The RX2 chip is a second-generation chip that was targeted specifically at achieving higher bandwidth than the original RX1 circuit. Consequently, there are substantial differences between the RX1 and RX2 designs. The RX2 LA was implemented with only Cherry–Hooper stages, eliminating the CML stages in the output block of the RX1 chip. An additional stage was added to the LA, bringing the total to six, to compensate for the reduced gain incurred by removing the CML stages. The LA in the RX2 design directly drives an inductively peaked differential output stage. Finally, although the differential TIA architecture was unchanged between the RX1 and RX2 circuits, the value of the transimpedance resistors were reduced by a factor of 2 in the RX2 design in an effort to improve the speed and, therefore, sensitivity at higher data rates, at the expense of reduced sensitivity at lower data rates.

Testing of the RX2 link proceeded in the same manner described previously for the RX1 link. Single-ended electrical
output eye diagrams produced by the RX 2 link under multiple operating conditions as a function of data rate are presented in Fig. 11. Fig. 11(a) shows data for the link operating with no TX predistortion; the eye diagram at 17.5 Gb/s is starting to close and is completely closed at 20 Gb/s. Fig. 11(b) and (c) was obtained on the RX2 link with TX predistortion at two different receiver operating points. The data in Fig. 11(a) and (b) were obtained with the RX2 receiver consuming 85 mW, while in Fig. 11(c), the RX2 operated at a lower power dissipation of 53 mW. The FFE TX was set to the same conditions as in Fig. 5(a) and (b) so the TX eye diagrams are not repeated here. As with the RX1 link, TX predistortion yields visible improvements to the total link performance and extends the operating range of the link to 20 Gb/s.

The receiver sensitivity characteristics of the RX2 link are shown in Fig. 12 for the same operating conditions used to obtain the eye diagrams of Fig. 11. The curves in Fig. 12(a) were taken with no TX predistortion at a receiver power dissipation of 85 mW, the data in (b) were obtained at the same RX setting but with TX predistortion enabled, and the characteristics in (c) were obtained at the lower RX power dissipation setting of 53 mW. Directly comparing Fig. 12(a) and (b), it is evident that under the same RX operating conditions, TX predistortion improves the sensitivity at $\text{BER} = 10^{-12}$ by more than 4 dB at 15 Gb/s and extends the capability of the link to 20 Gb/s.

Fig. 13 plots the timing margin for the RX2 link with and without TX predistortion at the 85 mW RX power setting. At 15 Gb/s and $\text{BER} = 10^{-11}$, predistortion yields an improvement of 0.09 UI (6 ps). Comparing the 17.5 Gb/s data illustrates a much larger improvement with TX predistortion: without it, the link does not operate below $\text{BER} = 10^{-9}$, while with predistortion, the link has a 0.46 UI (31 ps) horizontal eye opening at $\text{BER} = 10^{-11}$. At 20 Gb/s, with TX predistortion, the timing margin is 0.42 UI (28 ps) at $\text{BER} = 10^{-11}$.

Fig. 14 plots the sensitivity and timing margin penalties for transmission through up to 150 m of OM4 fiber. At 17.5 Gb/s, the sensitivity penalty incurred for 150 m transmission compared to back-to-back is <1.5 dB. Sensitivity measurements at 20 Gb/s were more challenging through fiber since the optical attenuator used for testing had to be eliminated to remove its insertion loss (~2 dB), but the penalty for 150 m transmission is no greater than 2 dB at 20 Gb/s. The timing margin curves in Fig. 12 indicate penalties of less than 0.05 UI (3 ps) and 0.1 UI (5 ps) for 150 m transmission at data rates of 17.5 Gb/s and 20 Gb/s, respectively.

The power efficiency of the RX2 link as a function of data rate was measured in the same manner as described previously for the RX1 link and the results are plotted in Fig. 15. As with the RX1 link, the power efficiency curve as a function of data rate is significantly flattened with TX pre-distortion. The RX2
Fig. 14. Sensitivity and timing margin data for the RX2 link operating with TX predistortion through up to 150 m of OM4 fiber. (a) Receiver sensitivity characteristics at 17.5 Gb/s. (b) Timing margin at 17.5 Gb/s. (c) Timing margin at 20 Gb/s. The RX2 chip power consumption was 85 mW for all the datasets.

Fig. 15. Power efficiency as a function of data rate for the RX2 link with and without TX predistortion.

Fig. 16. Block diagram of the double-equalized full link incorporating the RX3 receiver.

The last link we report here is shown in Fig. 16 and incorporates a receiver chip that will be referred to as RX3. As with the RX2 circuit, RX3 is a second generation design. Both RX2 and RX3 share the same differential TIA and use the same Cherry–Hooper stages in the LA. However, the RX3 chip only uses five Cherry–Hooper LA stages. Following the LA is an FFE circuit similar to the equalizer in the TX chip that was described in Section III.

The FFE output driver in the RX3 chip was specifically designed to improve signal integrity when driving through lossy package and printed circuit board (PCB) interconnects. In order to illustrate the capabilities of the RX3 chip, one of its outputs was connected through a 10″ long trace on a Nelco 4000 PCB as shown in Fig. 17. In this configuration, there are two links: the optical link between the TX and RX and the electrical link through the PCB between the RX output and the test equipment. In the data that follow, the total link power dissipation was 206 mW.

Fig. 18 presents eye diagrams at 20 Gb/s taken at the TX output, the directly probed RX output, and the RX output that traverses 10″ of PCB trace, for two link conditions: double equalized with both TX and RX FFE circuits enabled, and with no equalization.

VI. DOUBLE EQUALIZED FULL LINK WITH RECEIVER 3

The last link we report here is shown in Fig. 16 and incorporates a receiver chip that will be referred to as RX3. As with the RX2 circuit, RX3 is a second generation design. Both RX2 and RX3 share the same differential TIA and use the same Cherry–Hooper stages in the LA. However, the RX3 chip only uses five Cherry–Hooper LA stages. Following the LA is an FFE circuit similar to the equalizer in the TX chip that was described in Section III.

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Fig. 18 presents eye diagrams at 20 Gb/s taken at the TX output, the directly probed RX output, and the RX output that traverses 10″ of PCB trace, for two link conditions: double equalized with both TX and RX FFE circuits enabled, and with no equalization.
equalizers is dramatically illustrated by Fig. 18. Without equalization the link is broken, even at the directly probed RX output. With both TX and RX equalization enabled, the link is operational even with the extra 10 Gb/s PCB trace included.

Fig. 19 presents receiver sensitivity characteristics for the RX3 link. Fig. 19(a) plots the RX sensitivity at 15 Gb/s measured after the 10 Gb/s PCB trace under three different conditions: double equalization, transmitter equalization without receiver equalization, and receiver equalization without transmitter equalization. At 15 Gb/s, both TX and RX equalization is required to successfully close the optical and PCB electrical links. Fig. 19(b) plots the RX3 sensitivity characteristics measured after the PCB trace at multiple data rates up to 20 Gb/s.

VII. CONCLUSION

The effect of transmitter equalization is studied for three VCSEL-based multimode optical links. Unlike all previous works, the TX FFE settings are optimized for the entire link, including the receiver. Wide tuning range of the TX FFE allows strong predistortion of the VCSEL output, resulting in a dramatic improvement of all key metrics of the overall link performance. The example of the bandwidth-limited receiver RX1 described in Section IV is particularly striking: a link that struggled at 15 Gb/s was made to operate at 20 Gb/s. At 15 Gb/s, transmitter predistortion was shown to improve the sensitivity by >7 dB, horizontal eye opening by 3X, and the overall link efficiency by 2X. The demonstrated performance gains can be used to reliably build high-speed links using slower components, for example, receivers incorporating larger PDs.

We believe that the technique of transmitter pre-distortion demonstrated here offers a path to better performance and operating margin at all data rates and will be a powerful tool in extending the dominance of VCSEL-based interconnects for short-reach applications to data rates beyond 25 Gb/s.

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REFERENCES


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