Transmitter Pre-Distortion for Simultaneous Improvements in Bit-Rate, Sensitivity, Jitter, and Power Efficiency in 20 Gb/s CMOS-driven VCSEL Links


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DARPA Chip-to-chip Optical Interconnect (C2OI) Program
Equalization Required for Electrical Links at > 10 Gb/s

- 16” Tyco Backplane
- Impulse Response
- Transfer Function
- 9-Gb/s Equalization of 16” Tyco Channel

- Electrical I/O at 10 Gb/s and above require feature integrated serializer/deserializer blocks (PLL, CDR).
- Optical OE modules usually operate at 10 Gb/s.

- Power dissipation: 10.1mW from 1.0V power supply, BER < 10^-14 in center (PRBS7)

Basic Optical Link

- **Laser Driver:**
  - 100’s of mV in
  - 100’s of mV out

- **Fiber:**
  - Clean communications channel for short links (<100m)

- **Receiver:**
  - 10’s of μA in
  - 100’s of mV out
  - High gain*bandwidth extremely challenging in the front end: TIA and early LA stages
  - Analog circuits for maximum bandwidth in a given technology

*High gain typically refers to the gain in decibels (dB) which is a logarithmic ratio of power or voltage.
Driver with Feed-Forward Equalizer (FFE)

- Standard technique for electrical links to drive through PCBs, backplanes
- In optical modules, commonly included in RX output stages
- Incorporated here as part of the LDD circuit
Fiber is fairly well behaved

The “channel” to be equalized dominated by the VCSEL → PD → RX front-end (TIA plus first few LA stages)

- VCSEL bandwidth not necessarily easy to achieve, often reliability tradeoff
- Direct tradeoff between PD size and TIA Gain & BW
- Deterministic behavior of uniform OE and circuit components lends itself to equalization
- Particularly applicable to CMOS circuits
TX Pre-distortion set by monitoring BER and eye diagram at the receiver output: receiver power and bias unchanged

- TX equalization fully adjustable and can be completely disabled
- Best link performance when the VCSEL eye is overdriven to the point of visible distortion
- Pre-distorted eyes are the same for the RX2 link in the following slides

- VCSELs and PD provided by Emcore Corp.
  - 5μm diameter VCSEL, ~14 GHz bandwidth
  - 25μm diameter PD, 85 fF, 23 GHz bandwidth

Large Improvements in Sensitivity and Jitter

- Improvements at 15 Gb/s:
  - 7dB in sensitivity, 0.42 UI (28 ps) in eye-opening
- Extension of link speed to 20 Gb/s
- Better sensitivity at 17.5 Gb/s with pre-distortion than at 12.5 Gb/s without
**TX Pre-Distortion Link #2, with RX2**

- **Extension of link speed to 20Gb/s**
- **5.7pJ/bit total link power consumption while maintaining BER < 10^{-12} and >200mV_{ppd} at RX outputs**
- **> 4dB sensitivity improvement at 15Gb/s**
- **Reduction in fiber transmission penalties over 150m OM3 MMF (146mW link power setting):**
  - No EQ: 0.5dB @ 10Gb/s; 1dB @ 15Gb/s
  - With TX pre-distortion: < 0.5dB @ 15Gb/s; 1dB @ 17.5Gb/s; 1.5dB @ 20Gb/s

RX2 is the fastest 90-nm RX we have built → still shows dramatic improvements with TX pre-distortion

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**Same RX power dissipation**

**Lower RX power dissipation**
Improvement in Full-Link Power Efficiencies

- RX2 faster than RX1 \(\rightarrow\) RX1 shows more dramatic improvements at lower rates
- TX pre-distortion saves power at the receiver
- Pre-distorted links not only work more efficiently, but also with better performance and margin
- Record 5.7 pJ/bit efficiency for 20 Gb/s optical link

### Example power dissipation breakdown

<table>
<thead>
<tr>
<th>Component</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX PA</td>
<td>29.1</td>
</tr>
<tr>
<td>TX OS</td>
<td>21.4</td>
</tr>
<tr>
<td>VCSEL</td>
<td>10.5</td>
</tr>
<tr>
<td>TX Total</td>
<td>61</td>
</tr>
<tr>
<td>TX Equalizer</td>
<td>5.1</td>
</tr>
<tr>
<td>(included in total)</td>
<td></td>
</tr>
<tr>
<td>RX_TIA</td>
<td>14.5</td>
</tr>
<tr>
<td>RX_LA</td>
<td>33.4</td>
</tr>
<tr>
<td>RX_IO</td>
<td>4.5</td>
</tr>
<tr>
<td>RX Total</td>
<td>52.4</td>
</tr>
<tr>
<td>Link Total</td>
<td>113.4</td>
</tr>
</tbody>
</table>
Equalizing a Totally Different Link

- Sensitivity improvements: 4.5 dB @ 20 Gb/s, 4 dB @ 15 Gb/s
- Large reduction in jitter
- Equalizing the RX front-end → all other components capable of 40 Gb/s (mod. driver, MZ, Ge PD)
Summary & Outlook

- Driver with FFE used to heavily equalize optical links → transmitter pre-distortion
  - Used to improve total link performance, not TX output eye
- Enables simultaneous large improvements in maximum link operating speed, margin, jitter, and power efficiency
  - Demonstrated using multiple different receiver chips
- Demonstrated with both directly-modulated multimode VCSEL links and a singlemode link using a LiNbO$_3$ Mach-Zehnder modulator
- Enables record power efficiency for a full optical link at 20 Gb/s: 5.7 pJ/bit
- Front-end RX bandwidth is the primary factor compensated by TX pre-distortion
  - Pre-distortion can be used to alleviate RX design tradeoffs: PD size (capacitance)/TIA gain & bandwidth, LA gain & bandwidth
- Technique is well suited to highly-integrated Si photonic links with CMOS receiver circuits
- Well suited for AOCs
- Transmitter equalization is easier and more power efficient compared to conventional receiver equalization
- First demonstration with promising results, need to explore limits
  - Faster circuits needed to push beyond 20 Gb/s
  - Faster VCSELs will help, make equalization more effective at higher rates