Photonic Packaging in High-Throughput Microelectronic Assembly Lines for Cost-Efficiency and Scalability

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Abstract: We demonstrate silicon photonic packaging that can be fully exercised in existing microelectronic packaging facilities. We show low optical loss and point towards notably improved assembly cost and scalability in both volume and optical port-count.

OCIS codes: (130.3120) Integrated optics devices; (250.5300) Photonic integrated circuits

1. Introduction

Silicon photonics is based on leveraging microelectronics wafer fabrication facilities and processes to achieve a level of photonic integration complexity and affordability unrivaled by other approaches to optical systems. However, the mainstream approaches to optically connecting these silicon photonic chips to the outside world remain based on adaptations of legacy telecom practices. These can result in a package that is an order of magnitude more expensive than the chip itself, and which faces challenges in scalability in manufacturing volume and optical port count.

![Fig.1. Two implementations of photonic packaging in microelectronic tooling: direct fiber connection in (a)-(c), and a compliant polymer interface in (d)-(f). A polymer lid is assembled to a fiber-array stub in (a) for handling and fiber-pitch accuracy. The fiber stub and flipped laser chips are picked and placed on a photonic die with a standard high-throughput tool in (b)-(c). A polymer ribbon with integrated waveguides is assembled to a ferrule in (d). This polymer interface and flipped laser chips are assembled to a photonic die in (e)-(f). Self-alignment of fibers, polymer, and laser dies to the photonic die is required to leverage standard high-throughput microelectronics tools in (b) and (e).](image)
We argue that novel approaches to photonic packaging are required for silicon photonic technology to reach its full potential. We believe that the best way to disruptively reduce cost and improve scalability is to leverage existing microelectronics packaging facilities for photonic packaging, by the same token as microelectronic wafer fabrication facilities are leveraged for photonic chip fabrication. The enablement of high-throughput microelectronic tooling for photonic packaging comes with a number of challenges. In this paper, we present a high-level overview of how we overcame those obstacles to demonstrate approaches to photonic packaging that can be fully exercised in existing fully-automated, high-throughput, microelectronic packaging tools.

2. Overcoming limitations of microelectronic tooling

Two approaches to photonic packaging in microelectronic facilities are illustrated in Fig. 1. The corresponding experimental demonstrations are shown in Fig. 2. The first key challenge in employing microelectronic tools for photonic packaging is limited placement accuracy. Typical high-throughput tools show a placement accuracy of ± 10 um, which is insufficient for low-loss single-mode connections. Hence, self-alignment schemes are critical at every assembly step. Those are shown in Fig. 3 and need to be combined with optical designs that maximize assembly tolerances to achieve the desired performance. Our current optical interface designs are shown in Fig. 4. We employ butt coupling with metamaterial converters on chip as well as adiabatic coupling to chip. We avoid diffractive couplers as their bandwidth is inherently insufficient for coarse wavelength division multiplexing.

The second key challenge in employing microelectronic tools for photonic packaging is lack of flexibility in pick and place positioning. High-throughput tools are built to move at high speed in the plane of the chip first with a pressure sensitive movement being only possible downwards after in-plane positioning. Hence, one can position a fiber in a V-groove but not move it further in the plane of the chip for butting on a waveguide coupler. To overcome this limitation, the fiber butting to couplers in Fig. 1(b) is achieved with an angle-sliding base under the chip that trigonometrically transfers a portion of the vertical placing movement into a fiber butting force [1].

![Cross-sectional optical micrographs of the self-alignment schemes employed to bridge the gap between the ±10 um positioning accuracy of standard microelectronic tools and the required 1-2 um accuracy for photonics. (a) Grooves integrated on the photonic die self-align fibers at direct fiber connection to 1-2 um accuracy [1]. (b) Matching sets of polymer ridges and silicon grooves self-align the compliant interface to 1-2 um accuracy [3]. (c) At anneal, solder surface tension of connecting pads butt lithographically defined stops (on flipped chip and receiving die) for self-alignment with sub-micron capability [7].](image)
The direct fiber array assembly of Fig. 1(a)-(c) employs a polymer lid affixed to bare fibers to enable pick and place handling of the array with a vacuum pick tip and to maintain the fiber pitch accuracy to within the re-alignment capability of an integrated V-groove array on chip (Fig 3 (a)). The on-chip fiber coupler of Fig. 4 (a) and (d) was shown in [2] to offer a -1.3dB peak coupling efficiency to a standard cleaved fiber with 0.8 dB maximum penalty over a 100 nm bandwidth and all polarizations. The compliant polymer interface of Fig. 1(d)-(f) employs integrated polymer waveguides on a flexible ribbon to mechanically decouple the ferrule from the chip and avoid thermo-mechanical reliability issues such as fiber pistoning and other chip-package interaction. The self-alignment scheme of Fig. 3(b) has been shown to provide 1-2 um accuracy in [3-4]. The optical design was studied in [5] and employs butt coupling to fibers and adiabatic coupling to chip (Fig. 4 (b) and (e)). A peak transmission efficiency of -2.4 dB, from a fiber, through a polymer interface, to the chip, was reported in [6].

The InP die attach process requires even tighter alignment accuracy than fiber or polymer assembly due to the inherently smaller maximum mode size achievable on laser dies. We employ solder surface tension at anneal to push the InP die into alignment by butting lithographically defined alignment stops [7] (Fig. 3(c)). As the vertical alignment tolerances are tighter than the lateral alignment tolerances, we use an elongated mode as shown in Fig. 4(f).

3. Conclusion

We have demonstrated silicon photonic packaging that can be fully performed in standard microelectronic facilities. Self-alignment schemes with alignment-tolerant optical designs are critical to assembly in high-throughput tools.

4. References