IBM Silicon Nanophotonics Technology

Technology, Applications and Business perspective
IBM is adding to its semiconductor portfolio a CMOS Integrated Silicon Photonics technology which can support the design of electronics and optics on the same chip. The technology is cost optimized for bandwidths of up to 25Gbs per channel and can easily be deployed with WDM to achieve 100Gbs and more on single mode fiber.

IBM's clients are now considering a range of optical product solutions, such as a monolithic optical engine, optimally partitioned electronics with wafer level built-in-self-test (BIST), and even a companion silicon germanium chip to provide additional signal processing needs. IBM's evolving optical platform also includes an ecosystem of partners to provide clients with options for fiber connections, assembly, and optical module testing in the near future.

Today, IBM has an Eval PDK that was released nearly one year ago and there are reference designs in build. This talk will briefly overview this innovative silicon photonics technology and engagement in the OEM marketplace.
Technology

Differentiators

- Industry first sub-100nm monolithic Si Photonics
- Industry highest integration density
- Support multichannel 25Gbps optical engines
- Reach beyond 500m on duplex SMF with course WDM
- Flip-chip die attach for chip-on-board package
- Automated pick-and place packaging

Timeline

- Technology transferred to IBM Foundry in 2010
- Project transferred to IBM STG since 1Q 2013
- Qualification schedule: eval PDK (1Q13), α–PDK (2Q14), full technology qualification 2015
- Technology qual aligned with STG server and partners roadmaps
- In process of building vendor/supply chains and aligning partners and first adopters
Applications & Features

- Single die Multichannel Optical Engines 5Gbps – 25Gbps per channel
- 4-8 channel course WDM in PDK → scalability to higher data rates
- 90nm Digital library in PDK enables on die integration for microcontrollers, feedback regulators, equalizers & CDR
- PDK includes packaging structures for wafer level processing to accommodate fiber and laser attach
- COB flip-chip package allows smart partitioning of digital and analog functionalities – single chip vs multi-chip approaches depending on application
Engagement Options

- IBM Si Photonics technology in development for internal needs in high-end servers
- Joint development with partners
  - early access model
  - Reference design starting point
- Foundry model to provide volumes and service to clients
  - Standard design route (PDK, Cadence, LVS, DRC etc.)
  - Wafer-level foundry testing of standard qualified macros
  - First-level packaging (fiber and laser attach)

Example of wafer-level optical interface macro

Choice of wafer-level optical interface macros for automated packaging

- Pure-play foundry
  - Diced chips
- Photonics sub-assembly
  - Fiber/laser attach
- IBM advanced ASICs
  - Optical-electrical interconnect co-packaged

IBM Specialty Foundry, VT
Wafer Size: 200mm
Capacity: ~580,000 Wafers Per Year
Lithography nodes ranging from 500nm to 90nm
Diverse offerings focused on specialty foundry including SiGe 8HP & 9HP

In-line optical/ electrical test
Business engagement:

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